User Manual

Tektronix

VX4428
Quad ARINC-429
Transmitter/Receiver Module

070-9145-04

This document supports firmware version 1.00 and above.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to the Safety Summary prior to performing service.

CE

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Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

WARRANTY

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EC Declaration of Conformity

We

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The Netherlands

declare under sole responsibility that the

VX4428 and VX4428F and all options

meets the intent of Directive 89/336/EEC for Electromagnetic Compatibility. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Communities:

EN 55011 Class A Radiated and Conducted Emissions

EN 50081-1 Emissions:

EN 60555-2 AC Power Line Harmonic Emissions

EN 50082-1 Immunity:

IEC 801-2 Electrostatic Discharge Immunity
IEC 801-3 RF Electromagnetic Field Immunity
IEC 801-4 Electrical Fast Transient/Burst Immunity
IEC 801-5 Power Line Surge Immunity

To ensure compliance with EMC requirements this module must be installed in a mainframe which has backplane shields installed which comply with Rule B.7.45 of the VXIbus Specification. Only high quality shielded cables having a reliable, continuous outer shield (braid & foil) which has low impedance connections to shielded connector housings at both ends should be connected to this product.

ERRORS

See the E command (p. 3 - 26) for a full description of errors and error codes.

Fatal Errors

Fatal errors cause the VX4428 transmitter to disable the ARINC transmitter outputs. Any input from the card will return only the error code for the fatal error.

00	Message-RAM failure
01	Stack-RAM failure
02	Interrupt-controller failure

Nonfatal Errors

Nonfatal errors do not cause the VX4428 transmitter to totally suspend its operations. However, a hardware failure error within a channel permanently disables transmission from that channel until the error condition is cleared.

X0	Unrecognized Command
X1	Syntax
X2	Frame-header Missing
X3	ARINC-transmitter (Hardware failure error)
X4	Time-base (Hardware failure error)
X5	Channel Transmitting
X6	Delay-time
99	There are no errors remaining in the error buffer.

X = The channel affected by the error.

VX4428 Transmitter Quick Reference Guide

Numbers in parentheses refer to the page(s) in the Operating Manual.

SETUP

Be sure all switches are correctly set. (p. 1 - 5)
Follow Installation guidelines. (p. 2 - 1)
The default condition of the VX4428 transmitter after the completion of power-up self test is:

- Interrupts disabled.
- 100-kb/s bit rate for all channels.
- Transmitter outputs in null state.
- Channel 1 is the active channel.
- Power LED on.
- XMIT1-4 LEDs off.
- FAIL LED off if no Fatal errors have occurred during the power-up self-test.
- RFI LED off.
- ERR LED off if no self test errors are found.
- Channel-memory addresses at location 0.
- Trigger outputs/inputs for all channels disabled.
- Transmitters connected to the self-test data path.

LEDs

When on, the LEDs indicate the following:

PWR	power supplies functioning
FAILED	module failure
ERR	an error has been found in self test or programming
MSG	module is processing a VMEbus cycle
RFI	module has an unacknowledged VXIbus interrupt pending.
XMIT1 - XMIT4	the channel is transmitting data over the Mark 33 DITS bus.

SYSTEM COMMANDS

These non-data commands are initiated by the VX4428's commander. The following VXIbus Instrument Protocol commands will affect the VX4428:

ABORT NORMAL OPERATION	END NORMAL OPERATION
ASYNCHRONOUS MODE CONTROL	PROTOCOL ERROR QUERY
BEGIN NORMAL OPERATION	IDENTIFY COMMANDER
BYTE AVAILABLE	READ PROTOCOL
CLEAR	READ STATUS
CONTROL EVENT	TRIGGER
SET LOCK	CLEAR LOCK

COMMAND SYNTAX

Command protocol and syntax for the VX4428 transmitter is as follows (4 - 1, 4 - 2):

1. Binary data is in brackets [ ], using two hex characters for the binary value.
2. Any ASCII carriage return character sent or received is indicated by <CR>.
3. Any ASCII line feed character sent or received is indicated by <LF>.
4. Any other character shown is an ASCII character.
5. The write direction is data written TO the VX4428.
6. The read direction is data read back FROM the VX4428.

MODULE COMMANDS

A Address - sets an address in the selected channel's memory where the frame headers and ARINC data are to start being loaded, or the memory address from where the M (Memory Read) command is to start reading back message RAM. (3 - 20)

B Begin - starts transmission on a single channel or on all four channels. (3 - 21)

C Continue - continues transmission on a single channel after a STOP bit has been encountered in a header word. (3 - 23)

D Relay Close - connects the transmitter output(s) to the main output connectors. (3 - 25)

E Error - returns programming or hardware error codes. (3 - 26)

F Select Trigger Output - selects the front-panel and backplane trigger lines for the transmitter trigger output. (3 - 28)

I Interrupt Control - enables or disables the generation of system interrupts. (3 - 30)

K Reset - stops transmitter operation, and returns the VX4428 to its power-up state. (3 - 31)

L Length - specifies the number of header or ARINC data words to be transferred to the selected channel's memory. (3 - 32)

M Memory - retrieves data previously loaded by the user into the selected channel's memory. (3 - 33)

N Return ID - returns a string containing the module identification and software version to the system controller on its next request for input from the card. (3 - 34)

O Relay Open - connects the transmitter output(s) to the auxiliary output connector. (3 - 35)

P External Trigger Input Preset - initializes the transmitter(s) for external trigger input. (3 - 36)

Q Quit - stops transmission on a single channel, or on all channels, after a maximum of 17 words is sent by each transmitter. (3 - 38)

R Rate - specifies the period (in nanoseconds) of the bit-rate clock for the selected channel. (3 - 39)

S Select - selects the active channel for future commands. (3 - 40)

T Self Test - performs a functional self test of the complete VX4428 Module. (3 - 41)

V Voltage - specifies the output voltage level (normal, parametric high, parametric low, or parametric null) for the selected channel's transmitter. (3 - 42)

X Select External Trigger - selects the source for the external trigger input as either the front-panel inputs or the VXIbus TTL trigger lines. (3 - 43)

DATA TRANSMISSION FORMAT

Data output to a channel on the VX4428 is organized into frames, consisting of a single header word followed by one or more ARINC data words. Each header word or ARINC data word is four bytes long. The MSB of the fourth byte of each word specifies whether the word is a header word or an ARINC data word: 1 = header word; 0 = ARINC data word. A channel's frame storage is limited only by the RAM size of 32K words.

Table 1 shows the format of a standard header word (3 - 4), and Table 2 shows the format of an extended header word (3 - 7).

Each 32-bit ARINC data word is stored as four 8-bit bytes. The order in which each byte is transmitted and the ARINC data bits contained in each byte are shown in Table 3 (3 - 13).

LC Selectively changes one label in the list of capture labels for the Select-label Monitor Mode. (3 - 76)

LL Specifies a set of labels and secondary capture modes for Select-labels Mode.(3 - 77)

LM Specifies a set of data words to be used by the Monitor Mode to generate trigger outputs for the active channel. (3 - 79)

LP Sets the value of the limit parameter and the type of comparison for the Limit-check Mode. (3 - 81)

MM Selects one of the four primary capture modes and selects one of four sub-modes in the All-labels Mode. (3 - 83)

PR Sets the number of words to store before the trigger event has occurred for the Limit-check Mode. (3 - 85)

PT Sets the number of words to store after the trigger event has occurred for the Limit-check Mode. (3 - 86)

SD Specifies the data word return format as a single word or as one of the two block transfer modes for Monitor and Select-labels modes. (3 - 93)

SL Defines the capture label and secondary mode byte for the Limit-check mode. (3 - 95)

TD Sets whether <CR><LF> is added to the end of a data transfer. (3 - 97)

- **Command Order** - The order in which commands are given is critical and mode-dependent. If required commands are not present, or not in the correct sequence, errors may result. For details, see p. 3 - 60. In the following summary, an * indicates a required command.

All modes: RS (Reset), *MM (Main Mode), TR (Time-stamp Resolution), DS (Data Storage), *SC (Select Channel), TD (Terminate Data), ID (Return ID), BR (Bit Rate), IN (Interrupt)

Monitor Mode: SD (Select Data), *RE (Receiver Enable), LM (Load Masks)

Select-label Mode: SD (Select Data), *LL (Load Label), *RE (Receiver Enable)

Limit-check Mode: *SL (Set Label), *LP (Limit Parameters), *RE (Receiver Enable), PR (Pre-trigger), PT (Post-trigger)

VX4428 Receiver
Quick Reference Guide

Numbers in parentheses refer to the page(s) in the Operating Manual.

SETUP

Be sure all switches are correctly set. (p. 1 - 5)
Follow Installation guidelines. (p. 2 - 1)

The default condition of the VX4428 receiver after the completion of power-up self test is as follows:

General:
- Interrupts disabled.
- Trigger outputs disabled.
- Channel 1 selected.
- All channels in Monitor Mode.
- Data storage is time-stamp/error storage for all channels.
- All receivers are disabled.
- Power LED is on.
- ERR LED out if no errors are found during self-test.
- 1 ms time stamp resolution selected.
- <CR><LF> appended to the end of data transfers.
- Slow bit rate is selected for all channels (12-14.5 Kb/s).
- All receivers connected to the auxiliary input connector.

Mode-Specific:

Select-labels Mode:
- Capture label is label 0.
- Capture on label only.

Limit-check Mode:
- Capture label is label 0.
- Capture on label only.
- Limit comparison is equal.
- Limit parameter = 0.
- Pre-trigger and post-trigger = 0.

All-label Mode:
- Data is returned for label 0 only.

VXIbus Interface:
- FHS bit in the Response register is inactive (1).
- Read Ready bit in the Response register inactive (0).
- Request True interrupt enabled.
- ERR bit in the Response Register inactive (1).
- Logical address set to value on Logical Address switches.
- VXIbus interrupt out disabled.

LEDs When on, the LEDs indicate the following:

POWER	power supplies functioning
FAILED	module failure

ERR	an error has been found in self test or programming
RX1-4	data transmission occurring over the DITS bus connected to the channel's receiver
ERR1-4	channel's receiver enabled, error detected in the received data

SYSTEM COMMANDS

These non-data commands are initiated by the VX4428's commander. The following VXIbus Instrument Protocol commands will affect the VX4428:

ABORT NORMAL OPERATION	END NORMAL OPERATION
ASYNCHRONOUS MODE CONTROL	PROTOCOL ERROR QUERY
BEGIN NORMAL OPERATION	IDENTIFY COMMANDER
BYTE AVAILABLE	READ PROTOCOL
CLEAR	READ STATUS
CONTROL EVENT	TRIGGER
SET LOCK	CLEAR LOCK

COMMAND SYNTAX

Command protocol and syntax for the VX4428 receiver is as follows (4 - 1, 4 - 2):

1. Binary data is in brackets [ ], using two hex characters for the binary value.
2. Any ASCII carriage return character sent or received is indicated by <CR>.
3. Any ASCII line feed character sent or received is indicated by <LF>.
4. Any other character shown is an ASCII character.
5. The write direction is data written TO the VX4428.
6. The read direction is data read back FROM the VX4428.

MODES

To review modes and label format, see p. 3 - 45

- **Monitor Mode** - captures all data traffic on the ARINC-429 bus and stores the data sequentially, as a FIFO memory, in the VX4428's memory.
- **Select-labels Monitor Mode** - captures data based on a user-defined list of up to six ARINC-429 labels for each of four channels and stores the data sequentially, as a FIFO memory, in the VX4428's memory.
- **Limit-check Mode** - the VX4428 captures data for a single user-defined ARINC-429 label. Data is stored based on the trigger event and a user-defined pre- and post-trigger number of words.
- **All-label Mode** - the VX4428 captures and stores all ARINC-429 data received in separate memory locations based upon the label.

MODULE COMMANDS

Global Commands - function independently of the active channel.

CD	Clears the message RAM for one channel or all channels. (3 - 68)
CL	Clears the stored capture label(s) for Select-labels Monitor or Limit-check Modes. (3 - 69)
ER	Set to return error codes for all programming or hardware errors stored. (3 - 71)
EX	Set to return the Module's status byte. (3 - 73)
ID	Returns module identification and software revision. (3 - 74)
RC	Closes the source selection relay(s) to connect receiver(s) to the main input connector(s). (3 - 36, 3 - 87)
RD	Disables data reception for a single channel or for all four channels. (3 - 88)
RE	Enables data reception for a single channel or for all four channels. (3 - 89)
RO	Opens the source selection relay(s) to connect the receiver(s) to the auxiliary input connector(s). (3 - 90)
RS	Stops receiver operation and returns the module to its power-up state. (3 - 91)
SC	Selects the channel to be active for subsequent channel commands. (3 - 92)
ST	Perform a complete self test of the VX4428 Module. (3 - 96)
TE	defines whether the front panel and/or the backplane trigger output lines will be enabled/disabled. (3 - 98)
TR	Sets the time-stamp resolution value for all four channels. (3 - 102)
TS	Selects the trigger output lines for the front panel and the backplane trigger output lines. (3 - 100)

Channel-Specific Commands - affect only the currently selected channel.

BR	Selects a slow or fast bit rate for the received data. (3 - 64)
BT	Defines the list of labels whose data will be returned for the All-label Modes. (3 - 65)
DS	Sets the type of data words to be stored. (3 - 70)
IN	Enables or disables interrupts. (3 - 75)

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

Ground the Product. This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

The common terminal is at ground potential. Do not connect the common terminal to elevated voltages.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

VX4428
Quad ARINC-429
Transmitter/Receiver Module

Section 1
General Information and Specifications

Introduction

The VX4428 Quad ARINC-429 Transmitter/Receiver Module is a printed circuit board assembly for use in a mainframe conforming to the VXIbus Specification. The VX4428 Module transmits data onto and receives and analyzes data from the Mark 33 Digital Information Transfer System (DITS) found on commercial aircraft.

The VX4428 Module provides isolation relays and a self-test data path between the transmitter and receiver to provide a fully isolated test of both transmitter and receiver.

The VX4428 Module transmitter and receiver have Direct Memory Access (DMA) transfer capability to efficiently transfer data to and from the system controller. Either a programmable frame-by-frame interrupt, trigger output, or a readback of the address of the last ARINC word transmitted allows the user to synchronize updates to the card with the actual data transmission.

Transmitter

The VX4428 Module transmitter has four independent transmitters, each with an associated buffer memory for storing up to 32,768 ARINC-429 and control words for transmission on the DITS bus.

The VX4428 has trigger input and output capabilities. Trigger inputs can start transmission on any channel. Trigger outputs may be generated at the start of any frame for any channel. Trigger inputs and outputs are selected from the front panel and/or backplane TTLTRG lines.

The data stored in memory can be updated "in-progress" (while the VX4428 Module is transmitting). Transmission data in each memory is organized into "frames" consisting of a header word, for frame control, and one or more ARINC-429 data words. The header word controls the following:

- the frame transmission time (the time between the start of successive frames),
- the frame repeat count and control,
- the channel's transmission control (stop transmission with this frame; continue transmission from the start of memory),
- the interrupt and trigger output control for the channel,
- the frame's transmission parity, word length, and interword gap time.

The transmission voltage levels may be programmed independently for each channel to allow receiver parametric electrical testing.

The transmission bit rate for each channel is independently programmable from 122 bits/second (b/s) to 125 kb/s.

Receiver

The VX4428 Module receiver has four independent channels, each with an associated buffer memory for storing up to 32,000 ARINC-429 words (four bytes each) received on the DITS bus, for a total of 512,000 bytes of on-card memory. Programmable data capture modes offer great flexibility in testing and analysis. The receiver also has trigger output capabilities.

The receiver captures ARINC-429 data using one of the following four primary data-capture Activity modes. Each of the four channels is separately programmable.

- Monitor Mode

  In Monitor Mode, the receiver captures all ARINC-429 traffic received on the DITS bus and sequentially stores the captured data in the card's memory.

- Select-labels Monitor Mode

  In Select-labels Monitor Mode, the receiver stores data based on a user-defined list of up to six ARINC-429 labels for each of four channels. For each of the six user-defined labels, the Select-labels Monitor Mode also allows the data capture process to be further defined by the value of the source/destination-identifier (SDI) field and/or the sign/status-matrix (SSM) field. (Use of the SDI and SSM fields is defined in the ARINC-429 Specification.)

- Limit-check Mode

  In Limit-check Mode, the receiver will store ARINC-429 data based on a data limit condition for a single user-defined label, optionally qualified with the SDI and/or SSM field values. The module will automatically disable data reception after the data limit condition is met and the pre-defined number of data words following are stored.

- All-label Mode

  In All-label Mode, the receiver allocates one specific location in memory for all 256 possible ARINC-429 labels, optionally qualified with the SDI and/or SSM field value. The module will store only the latest data received for each label.

In each of the primary data-capture modes, the receiver allows data to be stored in one of the following three ways:

- ARINC-429 data words only.
- ARINC-429 data words plus time-stamp and error bytes.
- Only those ARINC-429 data words (including time-stamp and error bytes) in which an error has occurred.

Data stored in memory can be read while the receiver is receiving data with no loss of data. In Monitor and Select-label modes, the data is stored in a first-in-first-out (FIFO) structure. This means that reading data effectively frees up those storage locations for further data capture. In All-labels mode, memory is continuously updated to reflect the most current data. Older data is not retained by the module. In Limit-check mode, the most current data received is available to the system controller until the trigger event occurs. At that point, the number of words previously specified is stored and retained until the receiver is re-enabled, the mode for that channel is changed, or the data storage method is re-specified.

The Limit-check trigger event is also available as one or more of four front panel trigger outputs, or may be connected to multiple selected VXIbus backplane TTLTRG lines.

The independent time-stamp counters on each channel of the receiver are reset when the receiver is enabled. This provides an indication of the exact time when an ARINC-429 word was received (with respect to start of data collection), for any channel. The default setting for the programmable 16-bit counters is 1 ms, but they can be programmed from a 10 microsecond resolution to a 100 millisecond resolution, providing an overall count capability of up to 109 minutes before re-starting at zero again.

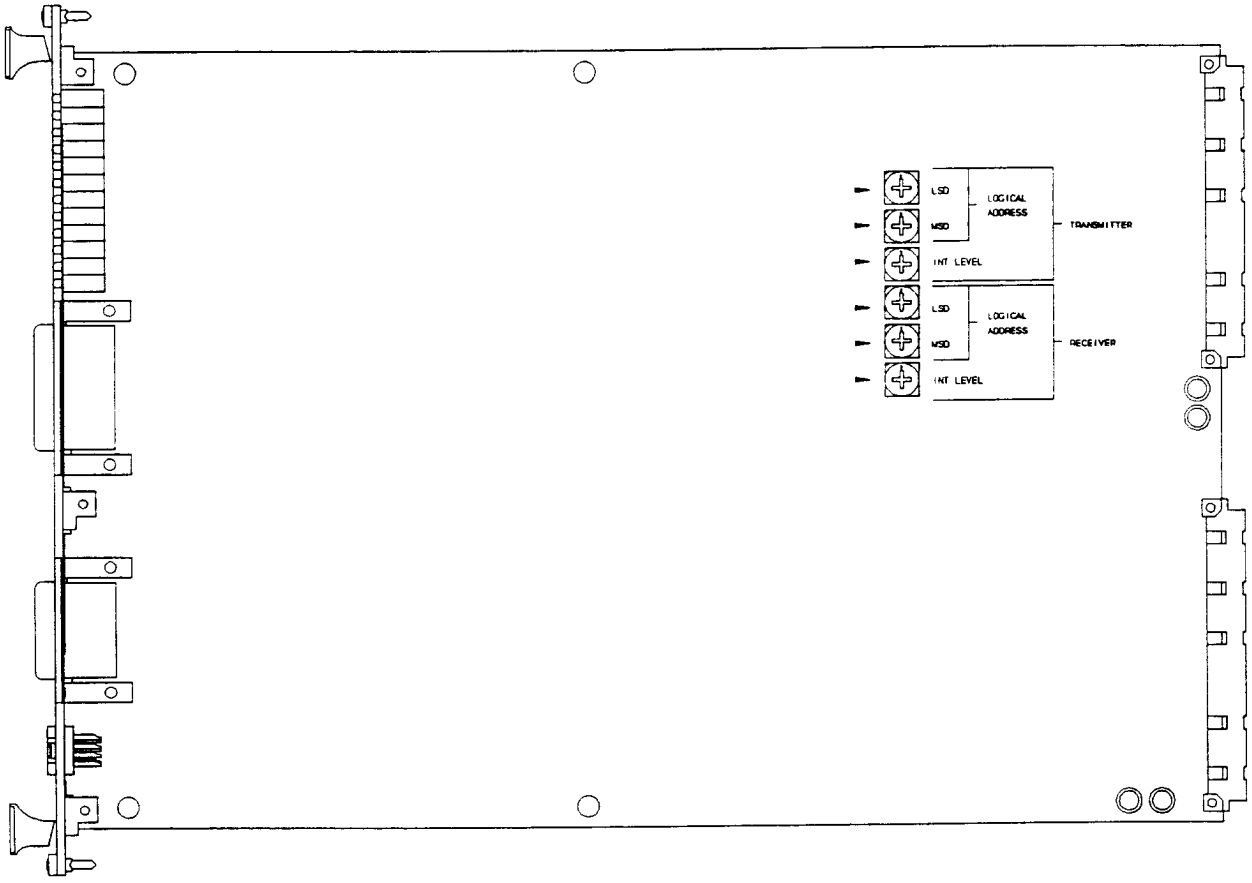


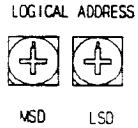
Figure 1: VX4428 Controls and Indicators

Controls And Indicators

The following controls and indicators are provided to select and display the functions of the VX4428 Module's operating environment. Since the transmitter and receiver portions of the VX4428 operate independently of each other and are separate VXI logical devices, they each have a separate set of Logical Address switches. All the switches must be set for proper operation. See Figures 1 and 2 for their physical locations.

Switches

Logical Address Switches



Each function module in a VXIbus System must be assigned a unique logical address, from 1 to 255 decimal. The base VMEbus address of the VX4428 transmitter or receiver is set to a value between 1 and FEh (254d) by two hexadecimal rotary switches. Align the desired switch position with the arrow on the module shield.

NOTE:
Even though the transmitter and receiver are on the same instrument, they must have separate logical addresses.

The actual physical address of the VX4428 transmitter or receiver is on a 64 byte boundary. If the switch representing the most significant digit (MSD) of the logical address is set to position X and the switch representing the least significant digit (LSD) of the logical address is set to position Y, then the base physical address of the VX4428 will be [(64d * XYh) + 49152d]. For example:

L.A.	MSD	LSD	Base Physical Addr. (d)
Ah	0	A	(64*10)+49152 = 49792d
15h	1	5	(64*21)+49152 = 50496d

where: L.A. = Logical Address
MSD = Most Significant Digit
LSD = Least Significant Digit

NOTE:
This module does not support VXIbus dynamic configuration.

IEEE-488 Address

Using the VX4428 Module in an IEEE-488 environment requires knowing the module's IEEE-488 address in order to program it. Different manufacturers of IEEE-488 interface

devices may have different algorithms for equating a logical address with an IEEE-488 address.

If the VX4428 is being used with a Tektronix/CDS IEEE-488 interface module, consult the operating manual of the Tektronix/CDS Resource Manager/IEEE-488 Interface Module being used.

NOTE:
Remember that the transmitter and receiver will have different IEEE-488 addresses.

If the VX4428 is being used in a MATE system, VXIbus logical addresses are converted to IEEE-488 addresses using the algorithm specified in the MATE IAC standard (MATE-STD-IAC). This algorithm is described in detail in the 73A-156 Operating Manual.

If the VX4428 is not being used with a Tektronix/CDS Resource Manager/IEEE-488 Interface Module, consult the operating manual of the IEEE-488 interface device being used for recommendations on setting the logical address.

VMEbus Interrupt Level Select Switch

Each function module in a VXIbus System can generate an interrupt on the VMEbus to request service from the interrupt handler located on its commander. When using the VX4428 with a Tektronix/CDS commander module, set the interrupt level to the same level as the interrupt handler on that commander. The VMEbus interrupt level on which the VX4428 transmitter or receiver generates interrupts is set by a BCD rotary switch. Align the desired switch position with the arrow on the module shield.

Valid Interrupt Level Select switch settings are 1 through 7, with setting 1 equivalent to level 1, etc. The level chosen should be the same as the level set on the VX4428's interrupt handler, typically the module's commander. Setting the switch to interrupt level 0 will disable the module's interrupts.

Interrupts are used by the module to return VXIbus Protocol Events to the module's commander. Refer to the Operation section for information on interrupts. The VXIbus Protocol Events supported by the module are listed in the Specifications section.

NOTE:
The transmitter and receiver may be set to the same interrupt level.

LEDs

The following LEDs are visible at the top of the VX4428 Module's front panel to indicate the status of the module's operation:

Power LEDs

These green LEDs are normally lit and are extinguished if the +5V power supply fails or if the transmitter or receiver +5V fuses blow. The transmitter and receiver have separate Power LEDs, labeled TXPWR and RXPWR.

Failed LEDs

These normally off red LEDs are lit whenever SYSFAIL* is asserted, indicating a module failure. Module failures include failure to correctly complete a self test, loss of a power rail, or failure of the module's central processor. The transmitter and receiver have separate Failed LEDs, labeled TXFAIL and RXFAIL.

If the module loses any of its power voltages, the Failed LED will be lit and SYSFAIL* asserted. A module power failure is indicated when the module's Power LED is extinguished.

Message LEDs

These green LEDs are normally off. When lit, it indicates that the module is processing a VMEbus cycle. The LED is controlled by circuitry that appears to stretch the length of the VMEbus cycle. For example, a five microsecond cycle will light the LED for approximately 0.2 seconds. The LED will remain lit if the module is being constantly addressed. The transmitter and receiver have separate Message LEDs, labeled TXMSG and RXMSG.

RFI LEDs

These normally off green LEDs are lit whenever the module has an un-acknowledged VXIbus interrupt pending. The LED will extinguish when a pending interrupt has been acknowledged by the module's controller. For an interrupt to be acknowledged, an interrupt acknowledge cycle must occur over the VXIbus backplane. The transmitter and receiver have separate RFI LEDs, labeled TXRFI and RXRFI.

XMIT1 - XMIT4 LEDs

When one of these LEDs is lit, it indicates the channel which is transmitting data over the Mark 33 DITS bus. They are labeled XMIT1 through XMIT4, for channels 1 through 4.

Error LEDs

These yellow LEDs are normally off. During self test, the Error LED blinks on and off. If an error is encountered during self test, the Error LED stays on continuously. The Error LED also comes on if an error is encountered during programming. The transmitter and receiver have separate Error LEDs, labeled TXERR and RXERR.

RX1 - RX4 LEDs

These green LEDs are lit when data reception is occurring over the Mark 33 DITS bus connected to the indicated channel receiver.

TX1 - TX4 LEDs

These green LEDs are lit when data transmission is occurring over the Mark 33 DITS bus connected to the indicated channel transmitter.

RXERR1 - RXERR4 LEDs

These yellow LEDs are lit when the indicated channel receiver is enabled and an error has been detected in the received data.

Destination Selection Relays

There is a destination selection relay on each of the four transmitters and receivers. The relays allow the VX4428 to switch the transmitters/receivers from the output connector to the self-test data path. All destination selection relays are in the open state (connected to the self-test data path) after power-up, commanded self test, reception of the Reset (RS) command, soft reset, and after reception of the VXI word serial Abort Normal Operations or End Normal Operations commands.

Fuses

The VX4428 Module has four fuses: one fuse for +5V for the transmitter, one fuse for +5V for the receiver, one fuse for +24V, and one fuse for -24V. The fuses protect the module in case of an accidental shorting of the power bus or any other situation where excessive current might be drawn.

If a +5V fuse opens, the VXIbus Resource Manager will be unable to assert SYSFAIL INHIBIT on the affected receiver or transmitter to disable SYSFAIL*.

If a +5V fuse opens, remove the fault before replacing the fuse. Replacement fuse information is given in the Specifications section.

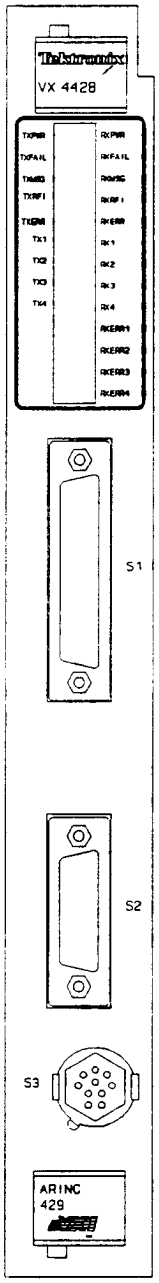


Figure 2: VX4428 Front Panel

BITE (Built-In Test Equipment)

The VX4428 Module provides commands which return the error code for any errors encountered during self test or programming.

Receivers

Extensive built in test equipment (BITE) is provided, including a self test of the RAM memories and the front end processors. Status LEDs at the front edge of the module provide a visual indication of data transmission, reception, and received-data errors on each channel.

Transmitters

Extensive self test capabilities are provided, including a wraparound check of each channel, self test of the RAM memory, and testing of the bit-rate and frame-rate counter/timers on the card. Error reporting provides readback of any errors encountered during self test or during programming. Status LEDs at the front edge of the card provide a visual indication of programming errors and data transmission on each channel.

Glossary

Note that certain terms used in this manual have very specific meanings in the context of a VXIbus System. These terms are defined in the VXIbus Glossary (Appendix C). In addition, the following terms specific to the VX4428 Module are defined:

active channel	The channel currently selected as the recipient for any following channel-specific commands.
DITS	Mark 33 Digital Information Transfer System.
empty frame	A frame which has no data words to be transmitted.
extended header	An extended header consists of eight 8-bit bytes containing the transmission control information of a standard header plus the frame repeat control.
FIFO	First-In/First-Out memory.
frame	A block of data for a transmitter consisting of a control header and ARINC 429 data words.
frame delay	The time between the transmission start of one frame and the transmission start of the following frame.
input	The data being sent FROM the card TO the system controller.

IWG Time	InterWord Gap time - The minimum number of bit times between the transmission of successive ARINC Words.
output	The data being sent TO the card FROM the system controller (typically commands and set-up parameters).
standard header	A standard header consists of four 8-bit bytes containing transmission control information for the ARINC 429 data words that follow.

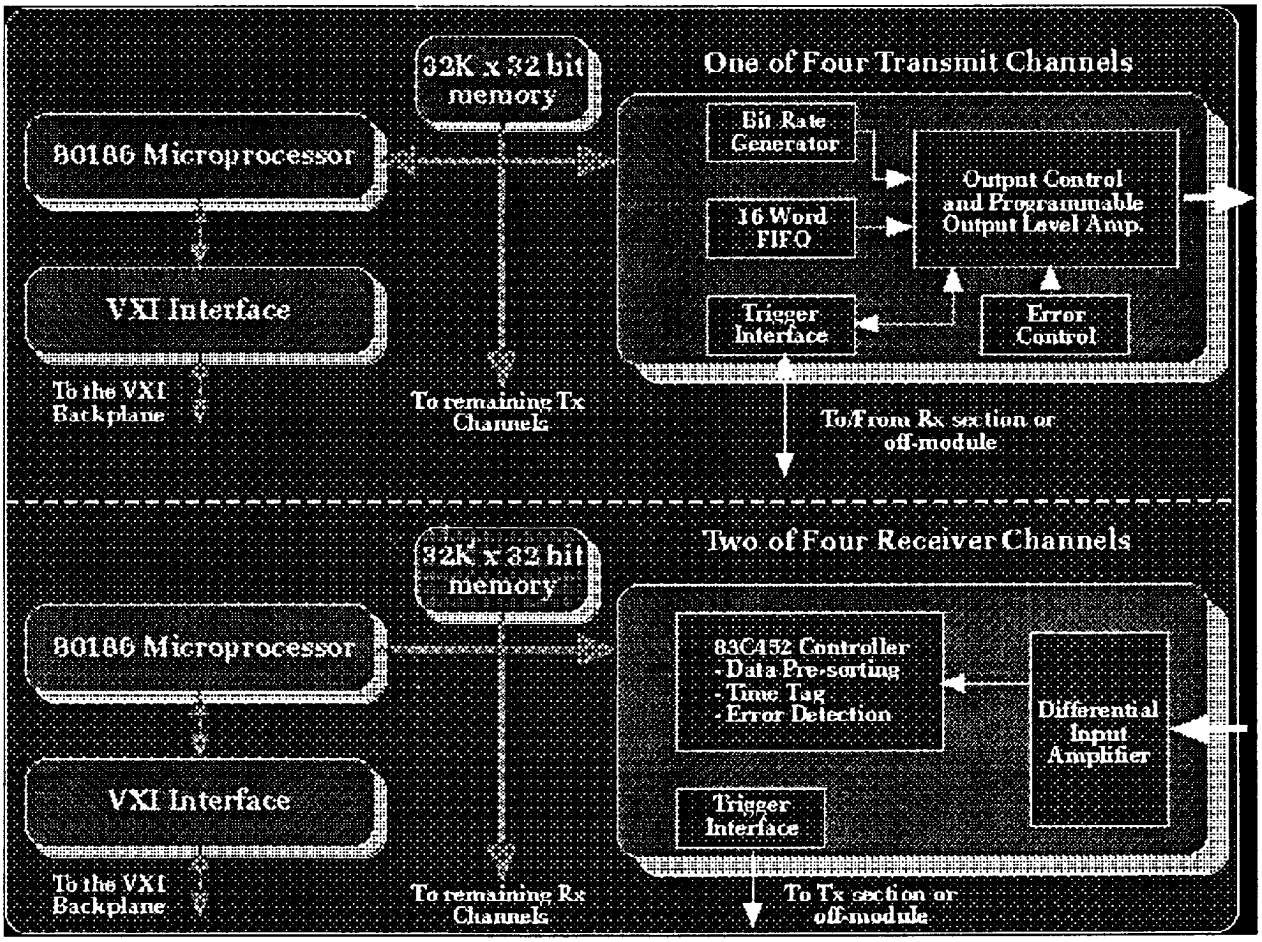


Figure 3: VX4428 Block Diagram

Specifications

** indicates a programmable feature*

TRANSMITTER

Configuration:	Quad (four channel) ARINC-429 Transmitter.
Processor:	1 - 80C186 (PLCC).
Coupling:	Connects directly to Mark 33 DITS bus.
RAM:	32K x 32-bit RAM memory associated with each channel for data and control instructions.
* Parity:	The VX4428 transmitter can generate odd or even parity, programmable on a frame-by-frame basis for each channel.
* DITS Word Format:	The transmitted DITS word can have 31, 32 or 33 bits, programmable on a frame-by-frame basis for each channel.
* Interword Gap:	Non-transmission time between words: two or four bit times, programmable on a frame-by-frame basis for each channel.
* Frame Interval:	Delay between the start of one frame and the start of the next frame: 5 ms to 4 s in 1-ms steps, programmable on a frame-by-frame basis for each channel. Accuracy: 1% - one bit-rate clock cycle ±150 µs, one channel transmitting; 1% - one bit-rate clock cycle ±500 µs, four channels transmitting.
* Bit-Rate Period:	8 µs to 8.19 ms in 250-ns steps, programmable independently for each channel.
* System Interrupts:	Programmable on a frame-by-frame basis for each channel to indicate the start of a frame.
* Output Triggers:	Programmable on a frame-by-frame basis for each channel to indicate the start of a frame.

ARINC Output (each channel)

Type Output:	Differential, ARINC Specification 429 compliant.

Preprogrammed Voltage Levels (no load):

Logic High and Low Voltage Levels

Parametric Normal Levels

Line A or B to Ground	±5 ± Accuracy.
Line A to B	±10 ± Accuracy.

Parametric High Levels

Line A or B to Ground	±6.5 ± Accuracy.
Line A to B	±13 ± Accuracy.

Parametric Low Levels

Line A or B to Ground	±3.25 ± Accuracy.
Line A to B	±6.50 ± Accuracy.

Parametric Null Levels

Line A or B to Ground	±1.25 ± Accuracy.
Line A to B	±2.50 ± Accuracy.

Logic Null Voltage Level

Line A or B to Ground	0 ±0.25 V.
Line A to B	0 ±0.50 V.

User Programmed Voltage Levels (no load): Line A or B to ground; 0 to 9.25 volts (.03628 volt steps) ± Accuracy.

Transmission Voltage Accuracy: (3% of programmed voltage) + 60 millivolts.

NOTE: All voltage levels are specified at no load. Each additional ARINC receiver has a loading effect on the output voltage. A single ideal ARINC receiver (also assuming no cable losses) depresses the transmitter output level by approximately 0.62% of the no load voltage. At the maximum 20 ARINC receivers, the output voltage level will be depressed by approximately 10.84% of the no load voltage. Allow for these voltage losses from the no load value in determining the desired transmission voltage level.

Rise/Fall Time: 16 kb/s to 125 kb/s: 1.5 ±0.5 µs.

122 kb/s to 15.936 kb/s: 10 ±5 µs.

Output Impedance: 75 ±5 ohm, balanced.

Drive Capability: 20 ARINC receivers (400 ohm maximum load).

Backplane
Trigger Outputs:

Type: TTL Open collector.
Drive: 48 milliamps.
Pulse width: 80 microseconds minimum; 120 microseconds maximum.

Front Panel
Trigger Outputs:

Type: TTL Open collector.
Drive: 48 milliamps.
Pulse width: 80 microseconds minimum; 120 microseconds maximum.

NOTE: The front panel trigger outputs require a pull-up at the destination in order to function properly.

Trigger Output To Transmission Start Delay:

1.5 bit times minimum, 2.5 bit times maximum.
A bit time is defined as the inverse of the bit rate frequency (1 / bit rate frequency).

Backplane
Trigger Inputs:

Type: TTL
Load: 0.2 milliamps maximum.
Pulse width: 250 nanoseconds minimum. The VXI Specification requires 10 nanosecond minimum, and some VXI TTLTRG sources may not be compatible with this input.

Front Panel
Trigger Inputs:

Type: TTL
Load: 8 milliamps maximum.
Pulse width: 250 nanoseconds minimum.

NOTE: The front panel trigger inputs have a 10,000 ohm pullup resistor installed on each input.

Auxiliary Outputs
(Channels 1 and 2)

Sync Out*:

Type output: TTL.
Drive: 6 standard TTL loads.
Sense: High while the channel is transmitting an ARINC-429 word.

CLK OUT *:

Type output: TTL.
Drive: 6 standard TTL loads.
Sense: Free-running clock at the channel's ARINC-429 data-transmission bit rate.
Duty cycle: 50%.

NRZ Data Out*:

Type output: TTL.
Drive: 6 standard TTL loads.
Sense: The channel's ARINC-429 output data in NRZ, high-true format. Data is valid on the falling edge of Data Clock Out.
Transmission order: LSB of ARINC-429 word first.

Data Clock Out*:
Type output: TTL.
Drive: 6 standard TTL loads.
Sense: NRZ data is valid on the falling edge of Data Clock Out. One output pulse for each of the channel's data bits transmitted.
Duty Cycle: 50%.
Rate: Equal to ARINC-429 bit rate.

* These signals are intended for use by the 53A-427 ARINC-429/561 Converter Module.

Power-Up:
The VX4428 transmitter powers up to the following states:
Interrupts disabled.
100-kb/s bit rate for all channels.
Transmitter outputs in null state.
Channel 1 is the active channel.
Power LED on.
XMIT1 LED off.
XMIT2 LED off.
XMIT3 LED off.
XMIT4 LED off.
FAIL LED off if no Fatal errors have occurred during the power-up self-test.
RFI LED off.
ERR LED off if no self test errors are found.
Channel-memory addresses at location 0.
Trigger outputs/inputs for all channels disabled.
Transmitters connected to the self-test data path.

Self Tests Performed:
Memory, time-base, and output-data tests (data output wrapped around to one of the processor's input ports prior to differential drive amplifiers).

RECEIVER

Configuration:
Quad ARINC-429 Receiver.

Processor:
1 - 80C186 (PLCC).
1 - 83C452 per channel.

Coupling:
Connects directly to Mark 33 DITS bus.

Valid Received Data Transmission Rates (ARINC-429):
High-speed (90 Kb/s to 110 Kb/s); Slow speed (12 Kb/s to 14.5 Kb/s). Consult factory for other bit rates.

Storage Capacity/Channel

Monitor Mode:
32,000 ARINC-429 words without time-stamp/error storage;
16,000 ARINC-429 words with time-stamp/error storage.

Select-labels Mode: 32,000 ARINC-429 words without time-stamp/error storage; 16,000 ARINC-429 words with time-stamp/error storage.

Limit-check Mode: 32,000 ARINC-429 words without time-stamp/error storage; 16,000 ARINC-429 words with time-stamp/error storage.

All-label Mode: 1 ARINC-429 word per label with or without time-stamp/error storage; or
1 ARINC-429 word per label and SDI and/or SSM bits with or without time-stamp/error storage.

Time-stamp Resolution (programmable):
10 µs to .65535 s in 10-µs steps.
100 µs to 6.5535 s in 100-µs steps.
1 ms to 65.535 s in 1-ms steps.
10 ms to 655.35 s in 10-ms steps.
100 ms to 6553.5 s in 100-ms steps.

IWG Time: High-speed (100-kb/s data rate): 35 µs, nominal.
Slow-speed (12-kb/s to 14.5-kb/s data rate): 266 µs, nominal.

VXIbus TTLTRG Outputs: Type: TTL Open collector.
Drive: 48 milliamps.
Pulse width: 150 nanoseconds minimum; 250 nanoseconds maximum.

Front Panel Trigger Outputs: Type: TTL Open collector.
Drive: 48 milliamps.
Pulse width: 300 nanoseconds minimum; 500 nanoseconds maximum.

NOTE: The front panel trigger outputs require a pull-up at the destination in order to function properly.

Power-up: The VX4428 receiver defaults to the following states on power-up:

General:
- Interrupts disabled.
- Trigger outputs disabled.
- All channels in Monitor Mode.
- Data storage is time-stamp/error storage for all channels.
- All receivers are disabled.
- Power LED is on.
- ERR LED out if no errors are found during self-test.
- 1 ms time stamp resolution selected.
- <CR><LF> appended to the end of data transfers.
- Slow bit rate is selected for all channels (12-14.5 Kb/s).
- All receivers are connected to the self-test data path.

Mode-Specific: Select-labels Mode:
- Capture label is label 0.
- Capture on label only.

Limit-check Mode:
Capture label is label 0.
Capture on label only.
Limit comparison is equal.
Limit parameter = 0.
Pre-trigger and post-trigger = 0.

All-label Mode:
Data is returned for label 0 only.

Self Tests Performed: Memory, front end processors test.

GENERAL

VXIbus Interface: Before the module's commander begins configuration of the module, it is in the following state:
FHS bit in the Response register is inactive (1).
Read Ready bit in the Response register inactive (0).
Request True interrupt enabled.
ERR bit in the Response Register inactive (1).
Logical address set to value on Logical Address switches.
VXIbus interrupt out disabled.

NOTE: The VXIbus interface state is prior to the module's commander beginning configuration of the module.

VXIbus Compatibility: Fully compatible with the VXIbus Specification for message-based instruments.

VXI Device Type: VXI message based instrument, Revision 1.4.

VXI Protocol: Word serial.

VXI Card Size: C size, one slot wide.

Module-Specific Commands: All module-specific commands and data are sent via the VXIbus Byte Available command. All module-specific commands are made up of ASCII characters. Module-specific data may be in either ASCII or binary format.

VMEbus Interface: Data transfer bus (DTB) slave - A16, D16 only.

Interrupt Level: Switch selectable, levels 1 (highest priority) through 7 (lowest).

Interrupt Acknowledge: D16; lower 8 bits returned are the logical address of the module.

VXIbus Commands Supported:

All VXIbus commands are accepted (e.g. DTACK* will be returned). The following commands have effect on this module; all other commands will cause an Unrecognized Command event:

ABORT NORMAL OPERATION
ASYNCHRONOUS MODE CONTROL
BEGIN NORMAL OPERATION
BYTE AVAILABLE (with or without END bit set)
BYTE REQUEST
CLEAR
CONTROL EVENT
END NORMAL OPERATION
PROTOCOL ERROR QUERY
IDENTIFY COMMANDER
READ PROTOCOL
READ STATUS
TRIGGER
SET LOCK
CLEAR LOCK

VXIbus Protocol Events Supported:

VXIbus events are returned via VME interrupts. The following event is supported and returned to the VX4428 Module's commander:

REQUEST TRUE (In IEEE-488 systems, this interrupt will cause a Service Request (SRQ) to be generated on the IEEE-488 bus.)

VXIbus Registers:

ID
Device Type
Status
Offset
Control
Logical Address
Protocol
Response
Data Low
See Appendix A for definition of register contents.

Power Requirements:

All required dc power is provided by the power supply in the VXIbus mainframe.

Voltage:

+5 Volt supply: 4.75 V dc to 5.25 V dc.
+24 Volt supply: +23.5 V dc to +24.5 V dc.
-24 Volt supply: -23.5 V dc to -24.5 V dc.

Current (Peak Module, I_{PM}):

5 Volt supply: Transmitter - 2.5 amps; Receiver - 1.2 amps.
+24 Volt supply: 220 mA.
-24 Volt supply: 200 mA.

Replacement Fuses:	+5V: Littlefuse P/N 273004 +24V: Littlefuse P/N 273001 -24V: Littlefuse P/N 273001
Cooling:	Provided by the fan in the VXIbus mainframe. Less than 10°C temperature rise with 1.97 liters/sec of air at a pressure drop of 0.22 mm of H_2O.
Temperature:	0°C to +50°C, operating. -40°C to +85°C, storage.
Humidity:	Less than 95% R.H. non-condensing, 0°C to +30°C. Less than 75% R.H. non-condensing, +31°C to +40°C. Less than 45% R.H. non-condensing, +41°C to +50°C.
VXIbus Radiated Emissions:	Complies with VXIbus Specification.
VXIbus Conducted Emissions:	Complies with VXIbus Specification.
Module Envelope Dimensions:	VXI C size. 262 mm x 353 mm x 30.5 mm (10.3 in x 13.9 in x 1.2 in)
Dimensions, Shipping:	When ordered with a Tektronix/CDS mainframe, the module is installed and secured in one of the instrument module slots (slots 1 - 12).
Weight:	1.76 kg (3.93 lbs.)
Weight, Shipping:	When ordered with a Tektronix/CDS mainframe, the module is installed and secured in one of the instrument module slots (slots 1 - 12). When ordered alone, shipping weight is: 2.21 kg (4.93 lb.)
Mounting Position:	Any orientation.
Mounting Location:	Installs in an instrument module slot (slots 1-12) of a C or D size VXIbus mainframe. (Refer to D size mainframe manual for information on required adapters.)
Front Panel Signal Connectors:	1 - 10-pin circular connector (socket) for the auxiliary outputs.
Recommended Cable or Connector:	1 - VX1786P Hooded Connector (10-pin circular, male). 1 - VX1783P Hooded Connector (15-pin D-type, male). 1 - VX1782P Hooded Connector (25-pin D-type, male).

Equipment Supplied: 1 - VX4428 Quad ARINC-429 Transmitter/Receiver Module.

Software Revision: V2.1

Section 2
Preparation For Use

Installation Requirements And Cautions

The VX4428 Module is a C size VXIbus instrument module and therefore may be installed in any C or D size VXIbus mainframe slot other than slot 0. If the module is being installed in a D size mainframe, consult the operating manual for the mainframe to determine how to install the module in that particular mainframe. Setting the module's Logical Address switch defines the module's programming address. Refer to the Controls and Indicators subsection for information on selecting and setting the module's logical address. To avoid confusion, it is recommended that the slot number and the logical address be the same.

Tools Required

The following tools are required for proper installation:

Slotted screwdriver set.

CAUTION

Note that there are two printed ejector handles on the card. To avoid installing the card incorrectly, make sure the ejector marked "VX4428" is at the top.

In order to maintain proper mainframe cooling, unused mainframe slots must be covered with the blank front panels supplied with the mainframe.

Based on the number of instrument modules ordered with the mainframe, blank front panels are supplied to cover all unused slots. Additional VXIbus C size single-slot and C size double-slot blank front panels can be ordered from your Tektronix supplier.

CAUTION

Verify that the mainframe is able to provide adequate cooling and power with this module installed. Refer to the mainframe Operating Manual for instructions.

If the VX4428 is used in a Tektronix/CDS VXI Mainframe, all VX4428 cooling requirements will be met.

CAUTION

If the VX4428 Module is inserted in a slot with any empty slots to the left of the module, the VME daisy-chain jumpers must be installed on the backplane in order for the VX4428 Module to operate properly. Check the manual of the mainframe being used for jumpering instructions.

Installation Procedure

CAUTION

The VX4428 Module is a piece of electronic equipment and therefore has some susceptibility to electrostatic damage (ESD). ESD precautions must be taken whenever the module is handled.

1) Record the revision level, serial number (located on the label on the top shield of the VX4428), and switch settings on the Installation Checklist. Only qualified personnel should perform this installation.

2) Verify that the switches are switched to the correct values.

3) Make sure power is off in the mainframe.

4) The module can now be inserted into one of the instrument slots of the mainframe.

5) Cable Installation -

   Use the appropriate cable to interface between the module I/O connector and the Unit Under Test (UUT).

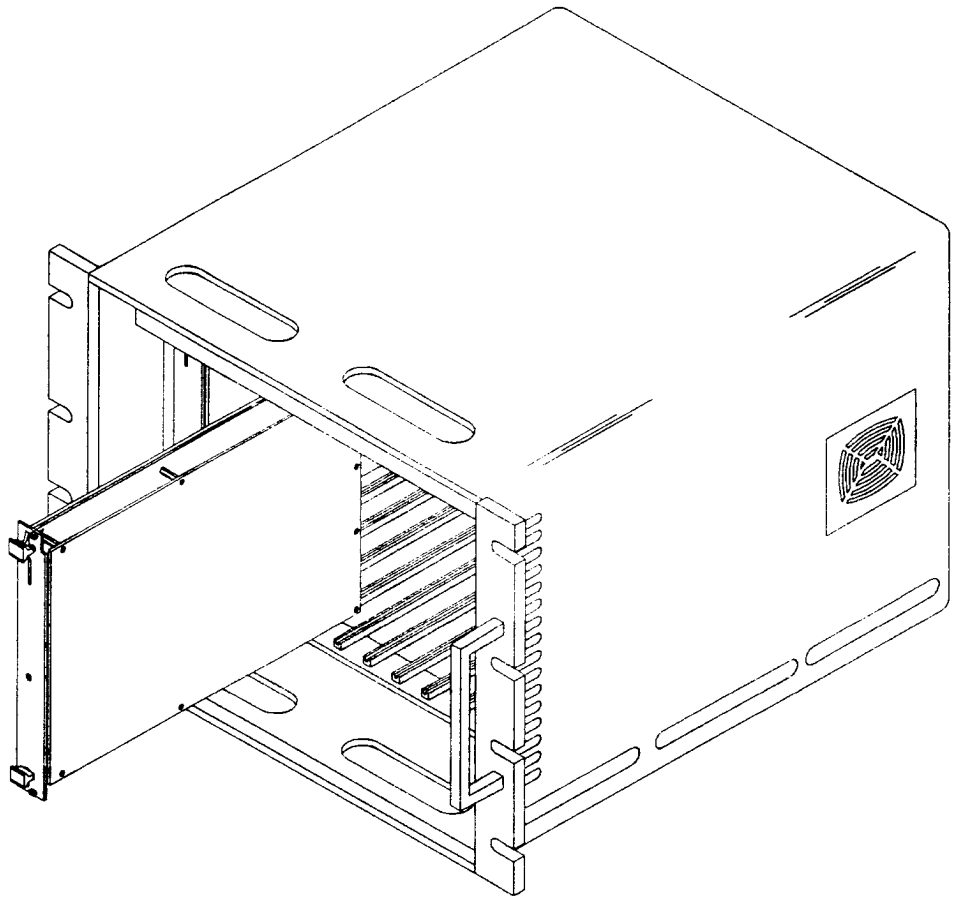


Figure 4: Module Installation

Installation Checklist

Installation parameters will vary depending on the mainframe being used. Be sure to consult the mainframe Operating Manual before installing and operating the module.

Revision Level: _____

Serial No.: _____

Mainframe Slot Number: _____

Transmitter Switch Settings:

VXIbus Logical Address Switch: _____

Interrupt Level Select Switch: _____

Receiver Switch Settings:

VXIbus Logical Address Switch: _____

Interrupt Level Select Switch: _____

Cable / Hooded Connector Installed:

_____

Performed by: _____ Date: _____

Section 3
Operation

Introduction

The VX4428 Quad ARINC-429 Transmitter/Receiver Module is a printed circuit board assembly for use in a mainframe conforming to the VXIbus Specification, such as the VX1400A C size mainframe used in the Tektronix/CDS IAC System. The VX4428 transmits data onto and receives and analyzes data from the Mark 33 Digital Information Transfer System (DITS) found on commercial aircraft.

The VX4428 Module has four independent transmitters, each with an associated buffer memory for storing up to 32,768 ARINC-429 and control words for transmission on the DITS bus. It also has four independent receivers, each with an associated buffer memory for storing up to 32,000 ARINC-429 words (four bytes each) received on the DITS bus, for a total of 512,000 bytes of memory. Programmable data capture modes offer great flexibility in testing and analysis.

The transmitter and receiver portions of the VX4428 have separate logical addresses and operate completely independently of each other. This is reflected in the organization of this section. Transmitter operation and commands are described first, followed by receiver operation and commands.

The VX4428 Module is programmed by ASCII characters issued from the system controller to the VX4428 Module via the module's VXIbus commander and the VXIbus mainframe backplane. The module is a VXIbus Message Based Device and communicates using the VXIbus Word Serial Protocol. Refer to the manual for the VXIbus device that will be the VX4428 Module's commander for details on the operation of that device.

Power-up

The VX4428 Module will complete its self tests and be ready for programming within five seconds after power-up. The VXIbus Resource Manager may add an additional one or two second delay. The Power LEDs will be on, and all other LEDs off. The MSG LEDs will blink during the power-up sequence as the VXIbus Resource Manager addresses all modules in the mainframe. The default condition of the module after power-up is described in the SYSFAIL, Self Test and Initialization subsection.

Transmitter Operation

The data stored in memory can be updated "in-progress" (while the VX4428 Module is transmitting). Transmission data in each memory is organized into "frames" consisting of a header word(s), for frame control, and one or more ARINC-429 data words. The

header word(s) controls the time interval between the start of one frame and the start of the next frame, and whether data in memory is to be transmitted once or continuously. To allow frame-by-frame testing of word-format protocol, the header word also controls parity (odd/even), word length (31, 32, or 33 bits), and the interword gap (two or four bit times) for the frame's ARINC-429 data words. The bit rate for each channel is programmable from 122 b/s to 125 kb/s. See the Data Transmission Format section for details.

The VX4428 Module has Direct Memory Access (DMA) transfer capability to efficiently accept data from the system controller. Using a system controller with DMA capability, the card supports memory updating in-progress when all four buses are operating at 100 KHz bit rates. Either a programmable frame-by-frame interrupt or a readback of the address of the last ARINC word transmitted allows the user to synchronize updates to the card with the actual data transmission.

The differential data output voltage levels may be programmed independently for each channel, to allow receiver parametric electrical testing.

Data Transmission Format

Data output to a channel on the VX4428 Module is organized into frames. Each frame consists of a header word followed by one or more ARINC data words. A channel can store multiple frames, limited only by the channel's RAM size of 32K words.

The first word in a channel's memory must be a header word; otherwise, an error is returned, and the channel will not start transmitting.

Each header word is either a standard header (four 8-bit bytes long) or an extended header (eight 8-bit bytes long). Each ARINC data word is four bytes long. The most significant bit of the fourth byte of the first header word or the fourth byte of each ARINC data word specifies whether the word is a header word or an ARINC data word:

a bit value of 1 specifies a header word
a bit value of 0 specifies an ARINC data word

NOTE: It is valid for a frame to contain zero ARINC data words. A frame with no data words (an empty frame) is treated as if the frame contains data words for the frame time, the repeat count in an extended header (if used), and the interrupt output. However, a trigger output will not be generated for an empty frame.

Header Word

The header word, which is output to an individual channel's memory as four or eight 8-bit bytes, contains the control information listed below:

Standard Header:

- The frame transmission time (the time between successive frames transmission start).

- The Frame's data transmission parity (odd or even), word length (31, 32, or 33 bits), and IWG Time (two or four bit times).
- Whether to generate a trigger output when the frame is transmitted.
- Whether to generate a VXIbus Request True Interrupt when the frame is transmitted or encountered (if the frame is empty).
- Whether to stop transmitting after the preceding frame's data has been transmitted.
- Whether to wrap around and continue transmitting from the start of memory or continue transmission with the data contained within the frame.
- The size of the header for the frame (four or eight 8-bit bytes).
- Whether to use the information contained in the second four 8-bit bytes.

Table 1 shows the format of a Standard header.

Extended Header:

- All of the functions of the Standard header.
- The number of times to repeat the frame.
- Whether to terminate the repeat count on reception of an external trigger.
- Whether to generate a VXIbus Request True Interrupt when the frame has been repeated the specified number of times.
- Whether to stop transmitting after the frame has been repeated the specified number of times.
- Whether to wrap around and continue transmitting from the start of memory or continue transmission with the next frame within memory after the frame has been repeated the specified number of times.

Table 2 shows the format of an Extended header.

TABLE 1: Standard Header Word Format for the VX4428 Transmitter

Output Byte	Bit Position							
	7	6	5	4	3	2	1	0
First	T3	T2	T1	T0	0	0	0	0
Second	T11	T10	T9	T8	T7	T6	T5	T4
Third	STOP	TMWRP	INT	TRG	IWG	LEN33	LEN31	EVNPAR
Fourth	HDR	0	0	0	0	0	0	0

A bit value of 1 means "high" or true, a bit value of 0 means "low" or false.

T0-T11

Bits T0 through T11 specify the frame's delay time. Setting particular T bits true causes the sum of the delay times for those bits to become the frame's delay time.

T Bit	Delay Time (ms)
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512
10	1024
11	2048

The maximum delay time which can be programmed (all T bits = 1) is 4.095 s; the minimum delay time which can be used is 5 ms. If a delay time of less than 5 ms is programmed for a frame, that frame's delay time automatically defaults to 5 ms.

NOTE: If the time required to transmit the ARINC data within a frame exceeds that frame's delay time, the following frame will not start transmission at the correct time. Instead, the following frame will start transmission at the completion of its own delay time. Since this causes all subsequent frames to lose synchronization

with their respective delay times, an error will be generated (error code X6, Delay-time error), and transmission will cease on the affected channel.

EVNPAR

EVNPAR specifies the parity of the current frame's ARINC data words:

0 odd parity; this is the normal ARINC parity.
1 even parity.

LEN33, LEN31

LEN33 and LEN31 specify the length of the current frame's ARINC data words:

LEN33	LEN31	Length
0	0	32-bit word selected. This is the length of a normal ARINC data word.
0	1	31-bit word selected.
1	0	33-bit word selected.
1	1	Illegal value.

When a 33-bit word is selected, bit 32 will be output as a 1, and bit 33 will be the parity bit. When a 31-bit word is selected, bit 31 will be the parity bit.

IWG

IWG specifies the interval between the transmission of successive ARINC words for the current frame:

0 four bit times between words; this is the normal IWG time for an ARINC data word.
1 two bit times between words.

TRG

TRG enables or disables the generation of a trigger output for the current frame. If the trigger output is enabled, a output trigger will be generated when the first bit of the first word for the frame is transmitted; this assumes that a trigger output line(s) has previously been selected for the channel.

0 a trigger output will not be generated for a frame.
1 a trigger output will be generated for a frame.

INT

INT enables or disables the generation of a VXIbus interrupt at the start of transmission of the current frame; this assumes that interrupts have been enabled previously with the I (Interrupt) command.

0 disables the generation of VXIbus interrupts for the current frame.
1 enables the generation of VXIbus interrupts for the current frame.

TMWRP

If the TMWRP (top-of-memory wrap) bit is set, the channel will continue transmitting from the start of memory after the preceding frame's data has been transmitted. The data contained in a frame with the TMWRP bit set will not be transmitted.

0 the data contained in this frame is transmitted.
1 transmission will continue with the first frame in memory; this frame's data is ignored.

STOP

If the STOP bit is set, the channel stops transmitting after the preceding frame's data has been transmitted. If the first header word in a channel's memory has the STOP bit set, the channel will not transmit, and VXIbus interrupts will not be generated for the channel.

0 the data contained in this frame is transmitted.
1 transmission will stop after the preceding frame's data has been transmitted.

HDR

The HDR bit must be set in order for a frame header to be recognized. If the HDR bit position is cleared, the word is assumed to be a ARINC data word.

0 this word is an ARINC data word.
1 this word is a frame header word.

TABLE 2: Extended Header Word Format for the VX4428 Transmitter

Output Byte	Bit Position							
	7	6	5	4	3	2	1	0
First	T3	T2	T1	T0	0	0	REPENB	EXTHDR
Second	T11	T10	T9	T8	T7	T6	T5	T4
Third	STOP	TMWRP	INT	TRG	IWG	LEN33	LEN31	EVNPAR
Fourth	HDR	0	0	0	0	0	0	0
Fifth	CNT7	CNT6	CNT5	CNT4	CNT3	CNT2	CNT1	CNT0
Sixth	CNT15	CNT14	CNT13	CNT12	CNT11	CNT10	CNT9	CNT8
Seventh	0	0	0	0	RWRP	EXT_TRG	RSTOP	RINT
Eighth	0	0	0	0	0	0	0	0

A bit value of 1 means "high" or true, a bit value of 0 means "low" or false.

EXTHDR

The EXTHDR bit indicates the presence of a Extended Header. When the EXTHDR bit is set, the header is assumed to be an Extended Header which uses eight bytes of storage.

0 this header is a standard 4-byte header.
1 this header is a 8-byte extended header.

REPENB

The REPENB bit indicates that the repeat control format contained in the second half of the header is to be used during transmission of this frame. If the REPENB bit is cleared and the EXTHDR bit is set, the second half of the extended header is ignored and transmission will continue with the first word following the second half of the extended header.

T0-T11

Bits T0 through T11 specify the frame's delay time. Setting particular T bits true causes the sum of the delay times for those bits to become the frame's delay time.

T Bit	Delay Time (ms)
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512
10	1024
11	2048

The maximum delay time which can be programmed (all T bits = 1) is 4.095 s; the minimum delay time which can be used is 5 ms. If a delay time of less than 5 ms is programmed for a frame, that frame's delay time automatically defaults to 5 ms.

NOTE: If the time required to transmit the ARINC data within a frame exceeds that frame's delay time, the following frame will not start transmission at the correct time. Instead, the following frame will start transmission at the completion of its own delay time. Since this causes all subsequent frames to lose synchronization with their respective delay times, an error will be generated (error code X6, Delay-time error), and transmission will cease on the affected channel.

NOTE: The frame delay time is examined only during the first time a frame is transmitted. During a repeat loop, all transmissions of the frame's data will be based upon the delay time used for the first transmission.

EVNPAR

EVNPAR specifies the parity of the current frame's ARINC data words:

0 specifies odd parity; this is the normal ARINC parity.
1 specifies even parity.

NOTE: The EVNPAR bit is examined when a header is first encountered. If the repeat count is enabled, the parity generated for the frame's data will be set the first time the frame is transmitted. All repeats of the frame's data will have the same parity.

LEN33, LEN31

LEN33 and LEN31 specify the length of the current frame's ARINC data words:

LEN33	LEN31	Length
0	0	32-bit word selected. This is the length of a normal ARINC data word.
0	1	31-bit word selected.
1	0	33-bit word selected.
1	1	Illegal value.

When a 33-bit word is selected, bit 32 will be output as a 1, and bit 33 will be the parity bit. When a 31-bit word is selected, bit 31 will be the parity bit.

NOTE: The LEN33 and LEN31 bits are examined when a header is first encountered. If the repeat count is enabled, the word length for the frame's data will be set the first time the frame is transmitted. All repeats of the frame's data will have the same word length.

IWG

IWG specifies the interval between the transmission of successive ARINC words for the current frame (inter-word gap):

0 specifies four bit times between words; this is the normal IWG time for an ARINC data word.
1 specifies two bit times between words.

NOTE: The IWG bit is examined when a header is first encountered. If the repeat count is enabled, the inter-word gap for the frame's data will be set the first time the frame is transmitted. All repeats of the frame's data will have the same inter-word gap length.

TRG

TRG enables or disables the generation of a trigger output for the current frame. If the trigger output is enabled, an output trigger will be generated when the first bit of the first word for the frame is transmitted; this assumes that a trigger output line(s) has previously been selected for the channel.

0 a trigger output will not be generated for a frame.
1 a trigger output will be generated for a frame.

NOTE: The TRG bit is examined when a header is first encountered. If the repeat count is enabled, the trigger output will be generated each time the frame's data is transmitted.

INT

INT enables or disables the generation of a VXIbus interrupt at the start of transmission of the current frame; this assumes that interrupts have been enabled previously with the I (Interrupt) command.

0 disables the generation of VXIbus interrupts for the current frame.
1 enables the generation of VXIbus interrupts for the current frame.

NOTE: The INT bit is examined when a header is first encountered. If the repeat count is enabled the INT bit is examined only during the first time the frame's data is transmitted; it is not examined while the frame is repeating.

TMWRP

If the TMWRP (top-of-memory wrap) bit is set, the channel will continue transmitting from the start of memory after the preceding frame's data has been transmitted. The data contained in a frame with the TMWRP bit set will not be transmitted.

0 the data contained in this frame is transmitted.
1 transmission will continue with the first frame in memory; this frame's data is ignored.

NOTE: The TMWRP bit is examined when a header is first encountered. If the repeat count is enabled, the TMWRP bit is examined only during the first time the frame's data is transmitted; it is not examined while the frame is repeating.

STOP

If the Stop bit is set, the channel stops transmitting after the preceding frame's data has been transmitted. If the first header word in a channel's memory has the STOP bit set, the channel will not transmit, and VXIbus interrupts will not be generated for the channel.

0 the data contained in this frame is transmitted.
1 transmission will stop after the preceding frame's data has been transmitted.

NOTE: The Stop is examined each time the frame is transmitted, including while the frame is repeating. This will cause the frame to be transmitted only once if a repeat frame with the Stop bit set is continued by use of the C (Continue) command.

HDR

The HDR bit must be set in order for a frame header to be recognized. If the HDR bit position is cleared, the word is assumed to be a ARINC data word.

0 this word is an ARINC data word.
1 this word is a frame header word.

CNT0-15

Bits CNT0 through CNT15 specify the number of times to repeat this frame's ARINC data words. Setting particular CNT bits true causes the sum of the count for those bits to become the repeat count. The repeat count is checked against the current number of times the frame has been repeated during every repeat of the frame's data. If the header's repeat count is less than or equal to the number of times the frame has been repeated, the repeat count for the frame will be terminated. This means that the repeat count can be changed while the channel is transmitting.

CNT Bit	Count Value
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512
10	1024
11	2048
12	4096
13	8192
14	16384
15	32768

The maximum repeat count which can be programmed (all CNT bits = 1) is 65535. If all of the CNT bits are zero, the frame's data will be repeated forever.

RINT

The RINT bit enables an interrupt to be generated at the start of transmission of the next frame when the repeat count has terminated. This interrupt will be generated only if the frame has been repeated the number of times set in the extended header. The reception of an external trigger event will not cause an interrupt to be generated (see EXT TRG bit definition). When both the RSTOP and RINT bits are set, the interrupt will

be generated approximately 2 milliseconds prior to the end of the last frame data transmission.

0 disable interrupt generation on repeat count termination.
1 enable interrupt generation on repeat count termination.

RSTOP

If the RSTOP bit is set, the channel will stop transmitting after the repeat count for the frame has been met. The frame transmitted when a Continue command is received will be the frame following the current frame.

0 continue with the next frame's data after the repeat count for this frame has terminated.
1 stop transmission after the repeat count for this frame has terminated.

EXT_TRG

If the EXT_TRG bit is set, the repeat frame will be terminated when an external trigger input is received. This assumes that an external trigger line has previously been selected. The repeat frame termination caused by an external trigger will bypass consideration of the following extended header bits, RINT and RSTOP. The RWRP bit will be acted upon as required.

0 ignore external trigger inputs during the repeat count.
1 terminate the repeat frame upon reception of an external trigger input. Transmission is continued with the next frame unless RWRP is set.

NOTE: The external trigger input will be cleared only when the channel starts transmission. If the P (Preset) command is used, the external trigger input which starts the channel's transmission will also cause the repeat count termination on external trigger input condition to be met on the first frame which has this condition enabled. Also, the external trigger input is monitored, and any trigger which is received at any time the channel is active is latched. Therefore the trigger input which causes the repeat count to terminate may have occurred during another frame's transmission.

RWRP

If the RWRP bit is set, the channel will continue transmission from the start of memory after the repeat has terminated.

0 continue with the next frame's data after the repeat count for this frame has terminated.
1 continue from the start of memory after the repeat count for this frame has terminated.

NOTE: When the RSTOP bit is set, transmission will cease when the current frame's repeat count has been met. When the RWRP bit is set, the first frame in memory will be executed when a C command is received.

ARINC Data Word

Each 32-bit ARINC data word is stored as four 8-bit bytes. The order in which each byte is transmitted and the ARINC data bits contained in each byte are shown in Table 3.

TABLE 3: Transmission Order for ARINC Data Words

First output byte:

Bit Position	7	6	5	4	3	2	1	0
ARINC Data Bits	1	2	3	4	5	6	7	8
Label	Most significant bit to least significant bit							

Second output byte:

Bit Position	7	6	5	4	3	2	1	0
ARINC Data Bits	16	15	14	13	12	11	10	9
Least Sig. Data Byte	Most significant bit to least significant bit							

Third output byte:

Bit Position	7	6	5	4	3	2	1	0
ARINC Data Bits	24	23	22	21	20	19	18	17
Mid Sig. Data Byte	Most significant bit to least significant bit							

Fourth output byte:

Bit Position	7	6	5	4	3	2	1	0
ARINC Data Bits	32	31	30	29	28	27	26	25

Most Sig. Data Byte: Value = 0 Most significant bit to least significant bit

BITS 1 Through 8

Bits 1 through 8 of an ARINC word are assigned as the word label by ARINC Specification 429.

BITS 31 Through 9

Bits 31 through 9 of an ARINC word are assigned as data by ARINC Specification 429.

BIT 32

Bit 32 of an ARINC data word (bit 7 of the fourth output byte) must be set to 0 to indicate to the VX4428 Module that this is an ARINC data word and not a header word. Bit 32 of the ARINC data word is assigned as the parity bit by ARINC Specification 429, but it is not necessary for the system controller to output a parity bit to the VX4428 Module. The module will generate the parity bit in the hardware; the generated parity bit is based on the parity defined in the frame's header word.

ARINC-429 Bus Data Transmission Order

The order in which the system controller sends the ARINC data word's bytes to the VX4428 Transmitter Module and the order of the bits in each byte are based on the needs of the programmer and the requirements of ARINC Specification 429. The order in which data is transmitted on the ARINC-429 bus is ARINC data bit 1 first, bit 2 second, etc., and bit 32 last.

Looking at how the four output bytes are defined in Table 3 above, bytes 1, 2, 3, and 4 are transmitted in that order. The most significant bit of byte 1, as output by the system controller, is transmitted first; the least significant bit of each of the other three bytes is transmitted first. This is because ARINC Specification 429 requires the order of transmission to be the label with the most significant bit first, followed by 24 bits of data with the least significant bit first.

The VX4428 Transmitter is designed to transmit the bits in the proper order, but to allow loading of the memory on the card with a label and data as they would be stored in the user's computer. Thus, the most significant bit of the label and of each data byte is the most significant bit as sent from the system controller to the card. This saves the programmer from having to write a routine to reverse the bit order of the label before it is sent to the VX4428 Module.

Controller-to-Module Data Transmission Order

Data is sent to the VX4428 transmitter as a sequence of header and ARINC data words. The order in which the data is sent to the VX4428 transmitter is shown in Table 4.

TABLE 4: Order of Data Transmission from System Controller to Module

Header or Data Word	VX4428 Transmitter Module Memory Address
Header 1	0
ARINC Data Word 1	1
.	
.	
.	
ARINC Data Word i	i
Header 2	i+1
ARINC Data Word 1	i+2
.	
.	
.	
ARINC Data Word j	i+j+1
Header 3	i+j+2
.	
.	
.	
Header Z*	number of ARINC data words and headers - 1.

* Header Z must be present, and either the STOP bit or the TMWRP bit must be set true. If Header Z is not present, the resulting operation is undefined.

The table shows only an example of the loading sequence for the transmitter. The frames shown could hold any number of ARINC data words, including zero. The minimum number of headers required for correct transmission is two. The extended header can be used any place a standard header is being used. The only change would be that the address for each header would include an extra address for the second half of the extended header.

In-Progress Updates

Internal to the VX4428 Transmitter Module, ARINC-429 data words are moved from the main memory in 8-ARINC-word blocks to a separate, high-speed, 16-ARINC-word, FIFO memory prior to transmission on the DITS data bus. The ARINC data words and frame headers contained in main memory can be updated in-progress (while the VX4428 Module is transmitting); these updates are limited by the following constraints:

1. Updates to the frame header currently being transmitted are not effective until the next pass through the transmission list.

2. Updates to the first eight ARINC data words of a frame that is within 5 ms of being transmitted are not sent on the bus until the next pass through the transmission list.

3. Updates to the next eight ARINC data words of the frame currently being transmitted are not sent on the bus until the next pass through the transmission list.

4. The header word following a frame whose last data word has already been transmitted cannot be changed to an ARINC data word.

When updating a channel's memory during transmission, there are two ways of determining where the channel is in its transmission sequence:

1. Requesting input from the VX4428 Transmitter Module automatically provides the next memory address to be accessed by the selected channel; the address is always five ASCII digits with leading zeros. This feature is available at all times except when an error-code return is requested (see Operation section, E command).

2. The INT bit in the header can generate an interrupt to the system controller at the start of any user-selected frame.

Interrupt Generation

When enabled, the interrupt generation capability of the VX4428 Transmitter Module will generate a VXIbus Request True interrupt to its controller when a frame with the interrupt bit set in the header word is encountered during transmission.

If the module encounters a new interrupt condition after an interrupt has been generated, a new interrupt will be generated after the initial interrupt has been

acknowledged. In order for a new interrupt to be generated, the present interrupt must be acknowledged by both a VXIbus interrupt acknowledge cycle and a serial poll (word serial Read STB command).

After the VXIbus interrupt acknowledge cycle has occurred, the serial poll will return an 8-bit byte of data in the following format:

	Serial Poll Byte							
Bit Position	7	6	5	4	3	2	1	0
	0	1	1	1	chan 4	chan 3	chan 2	chan 1

Channels 1-4, when active (1), indicates which channel(s) are generating the interrupt.

Trigger Output Generation

When the trigger bit in the header is set, a trigger output will be generated to the user-selected VXIbus backplane TTL Trigger line and/or the front-panel trigger output line when the first bit of the frame is transmitted. A trigger output will not be generated if the frame contains no data to be transmitted (an empty frame).

System Commands

These low-level commands are typically sent by the module's commander, transparent to the user of the module. An exception is the Read Status command, which is sent whenever a Serial Poll on an IEEE-488 system is performed. Most commanders or Slot 0 devices have specific ASCII commands which will cause them to send one of these low-level commands to a specified instrument. Refer to the Operating Manual of the commander or Slot 0 device for information on these commands.

Module Commands

A summary of the VX4428's transmitter commands is listed below. This is followed by detailed descriptions of each of the commands.

Command Syntax

Command protocol and syntax for the VX4428 transmitter are as follows:

1) If a character is not enclosed by brackets, that character itself is sent, otherwise:

   [ ] encloses the symbol for the actual argument to be sent. These argument symbols are defined under each command heading.

   <CR> indicates a carriage return.

   <LF> indicates a line feed.

2) Any character may be sent in either upper or lower case form.

3) Any of the following white space characters:
00 hex through 2F hex
3A hex through 40 hex
5B hex through 60 hex
7B hex through FF hex

are allowed at any time as spacers, except when binary data is being transferred.

4) When binary data is referenced as a command parameter it is intended to be sent as an 8-bit binary value.

For example, the numeric character '3' is represented in 8-bit ASCII as "00110011", with each zero (0) or one (1) representing a single bit from high bit position to low bit position. In straight 8-bit binary the value of '3' is represented as "00000011". When a binary value is required it is the second format which must be used.

5) Any character not explicitly defined as binary is to be sent in ASCII.

Summary

Detailed descriptions of each command (in alphabetical order) are given following the summary below.

Command Action

A Set Address - sets an address in the active channel's memory where the frame headers and ARINC data are to start being loaded, or the memory address from where the M (Read Memory) command is to start reading back message RAM.

B Begin Transmission - starts transmission on a single channel or on all four channels.

C Continue Transmission - continues transmission on a single channel or all channels after a STOP bit has been encountered in a header word.

D Relay Close - connects the transmitter output(s) to the output connector.

E Error Return - returns programming or hardware error codes.

F Trigger Output - selects the front-panel and backplane trigger lines for the transmitter trigger output.

I Interrupt Control - enables or disables the generation of VXI interrupts by the transmitter module.

K Reset - stops transmitter operation, and returns the VX4428 transmitter to its power-up state.

L Load Memory - specifies the number of header or ARINC data words to be transferred to the selected channel's memory.

M Read Memory - retrieves data previously loaded by the user into the selected channel's memory.

N ID Return - returns the transmitter ID string.

O Relay Open - connects the transmitter output(s) to the internal self-test data path.

P Trigger Preset - initializes the transmitter(s) for external trigger input.

Q Quit Transmission - stops transmission on a single channel, or on all channels, after a maximum of 17 words is sent by each transmitter.

R Bit Rate - specifies the period (in nanoseconds) of the bit-rate clock for the active channel.

S Select Active Channel - selects the active channel for future commands.

T Self Test - performs a functional self test of the complete VX4428 transmitter.

V Voltage Level - specifies the output voltage level (normal, parametric high, parametric low, or parametric null) for the active channel's transmitter.

X Trigger Input - selects the source for the external trigger input as either the front-panel inputs or the VXIbus TTL trigger lines.

A detailed description of each command, in alphabetical order, is given on the following pages.

Command Descriptions

Command: A (Set Address)

Syntax: [addr] A

Purpose: The A (Set Address) command sets the starting memory address for the active channel. The address is used by the L (Load Memory) and M (Read Memory) commands as the starting address to load memory or read back the stored data.

Description: [addr] is a 1- to 5-digit decimal integer, from 0 to 32767, that specifies the value to load as the load/read starting address for the active channel. If [addr] is omitted, the address is set to 0. A VX4428 transmitter memory location is 32 bits wide and contains one complete header word or ARINC data word.

The A command is used at the beginning of a data transfer only if the current address for the active channel needs to be modified. The A command is not needed for loading or reading consecutive address since the VX4428 transmitter automatically increments the address after every word is transferred.

The A command will not affect the read address of a currently active M command and will not be the load address of a following L command if the M command completes before the L command is received. The M command completion will set the load address for the L command to the next address in memory after the last word transferred by the M command.

NOTE: The first header word loaded and its associated ARINC data words must start at memory address 0, and be contiguous. If they are loaded into non-contiguous memory locations, the random data in the non-programmed locations will be either transmitted on the ARINC-429 bus or interpreted as a header word. Data loading always begins with byte 1 of a word.

Example: 14000 A programs the load/read starting address of the active channel to 14000.

Errors: A Syntax error will result if an out-of-range value is specified for the [addr] parameter.

If a Syntax error is generated when the command is received, the command will be ignored.

Command: B (Begin Transmission)

Syntax: [chan]B

Purpose: The B (Begin Transmission) command starts transmission on the specified channels, starting from the first location in memory.

Description: [chan] is a 1-digit decimal integer that specifies the following:

[chan]	Begin Transmission on Channel(s)
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

The B command has no effect on channels already transmitting or channels preset for external trigger input (see the P command) which are waiting for an external trigger to start transmission.

The first frame control bits for each channel will be tested and acted on in the following sequence (assuming that no errors are generated during the command execution):

1. If the Interrupt bit is set, a VXIbus interrupt will be generated at the completion of the command.

2. If the Stop bit is set, transmission will not start, but the C command will be enabled for the channel. The B command will continue with the next channel to be started.

3. If the Trigger bit is set, the trigger output will be generated when the first bit is transmitted. (If the first frame is an empty frame, the trigger output will not be generated.) The B command will continue with the next channel to be started.

The B command will also clear the external trigger input used by the extended header prior to starting transmission.

CAUTION:

The B command will reset the channels to be started prior to starting transmission. Be sure that all data has been transmitted after a Stop bit or a Q command.

Examples:

1. 4B starts transmission on channel 4.

2. 0B (or simply B) starts transmission on all four channels.

Errors:

A Syntax error will result if an out-of-range value is specified for the [chan] parameter.

A Channel Transmitting error will result if the command is issued to a channel currently transmitting or waiting for an external trigger to start transmission.

A Frame-header Missing Error will result if the command is issued to a channel which does not have a header loaded into the first location in memory.

If a Syntax error is generated when the command is received, the command will be ignored. If a Channel Transmitting or Frame-header Missing error is generated, the channel which encountered the error will not start transmission.

Command: C (Continue Transmission)

Syntax: [chan]C

Purpose: The C (Continue Transmission) command continues transmission on the defined channel(s) after a STOP bit has been encountered in a header word.

Description: [chan] is a 1-digit decimal integer that specifies the following:

[chan]	Transmission Continued on Channel
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

If a C command is issued for a channel which has not encountered a Stop bit in a header word, the command has no effect on that channel.

The first frame's control bits for each channel will be tested and acted on in the following sequence (assuming that no errors are generated during the command execution):

1. If the Wrap bit is set the control bit search will continue at the first frame in memory.

2. If the Interrupt bit is set, a VXIbus interrupt will be generated at the completion of the command.

3. If the channel has wrapped in memory to the first frame, then the Stop bit is checked, otherwise, this step is skipped. If the stop bit is set, transmission will not start, but the C command will be enabled for the channel. The C command will continue with the next channel to be started.

4. If the Trigger bit is set, the trigger output will be generated when the first bit is transmitted. (If the frame is an empty frame, the trigger output will not be generated.) The C command will continue with the next channel to be started.

The C command will also clear the external trigger input used by the extended header prior to starting transmission. When using an extended header, the Continue command will continue with the next frame after the extended header frame.

Within the VX4428, data for each channel is moved from main memory in blocks of eight ARINC words to a separate, 16-ARINC-word, high-speed, FIFO memory which drives a given channel's DITS data bus. Once a channel has halted transmission due to encountering a header word's Stop bit, a C command should not be issued until the FIFO memory has emptied. To determine when to issue the C command, proceed as follows:

1. Select the desired channel using an S command, and request input from the card. The address of the current memory locations being processed will be returned.

2. When the returned current memory location is equal to the location of the header word containing the Stop bit, then wait for 576 times the programmed bit rate before issuing the C command.

Examples:

1. 4C continues transmission on channel 4.

2. 0C (or simply C) continues transmission on all four channels.

Errors:

A Syntax error will result if an out-of-range value is specified for the [chan] parameter.

A Frame-header Missing error will result if the command is issued to a channel which does not have a header at the current location in memory (This error will be generated for the first location if the wrap bit is set for the current location).

If a Syntax error is generated when the command is received, the command will be ignored. If a Frame-header Missing error is generated, the channel which encountered the error will not start transmission.

Command: D (Relay Close)

Syntax: [chan]D

Purpose: The D (Relay Close) command will close the destination selection relays to connect the transmitters to the output connector for the specified channel(s).

Description: [chan] is a 1-digit decimal integer (or blank) that specifies the channel or channels affected by the D command as follows:

[chan]	Channel(s) Affected
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

NOTE: After the D command has been executed, there will be a 10 millisecond delay to allow the relays to settle before the module will be ready for subsequent commands.

CAUTION:

The relays can be opened (with the O command) or closed (with the D command) while the channels are transmitting over the DITS bus. If the relays change position while data transmission is occurring on the DITS bus, transmitted data corruption may occur. It is recommended that the Relay Close command be used only while data transmission is not occurring.

Examples:

1. D or 0D will connect all four channels to the output connectors.

2. 3D will connect channel 3 to the output connector.

Errors: A Syntax error will result if an out-of-range value is specified for the [chan] parameter.

If a Syntax error is generated when the command is received, the command will be ignored.

Command: E (Error Return)

Syntax: E

Purpose: The E (Error Return) command prepares the VX4428 transmitter to return programming or hardware error codes to the system controller on its next request for input from the card.

Description: Each returned error code consists of two ASCII characters followed by <CR><LF>. After an E command is sent, the VX4428 transmitter continues to return error codes on each input request from the system controller until error code 99 (no additional errors to report) is returned. Additional requests for input (after error code 99 is returned) return the address of the last transmitted word from the active channel. The ERR LED will not go out until the error code 99 is read.

If an E command is issued and no errors are found, only error code 99 is returned. Because the error buffer can store a maximum of 16 errors, only the first 16 errors are returned; any additional errors are lost. Errors are returned in the order in which they are encountered.

The E command will be aborted by receiving a M command or the VXIbus word serial Clear command. If the E command is aborted, only those error codes which were completely read (including the <CR><LF>) will be cleared from the error buffer. Any error codes not read will remain in the error buffer and the error LED will not go out.

Errors: A Syntax error will result if any numerical value immediately precedes the E command.

If a Syntax error is generated when the command is received, the command will be ignored.

Error Codes: "Fatal" errors cause the VX4428 transmitter to disable the ARINC transmitter outputs, set the SYSFAIL* VXIbus line, clear the Passed bit in the VXIbus status register, and turn the Fail LED on. The VX4428 transmitter will then accept commands from the system controller, but will not perform functions for any commands. Any input from the card will return only the error code for the fatal error.

Fatal Errors

Error Code	Description
00	Message-RAM failure
01	Stack-RAM failure
02	Interrupt-controller failure

"Nonfatal" errors do not cause the VX4428 transmitter to totally suspend its operations. However, a hardware failure error within a channel permanently disables transmission from that channel until the error condition is cleared.

Nonfatal Errors X = The channel affected by the error.

Error Codes	Description
X0	Unrecognized Command - generated when an invalid command is received.
X1	Syntax - caused when a command is issued which has errors in the command parameters.
X2	Frame-header Missing - the first location in memory is not a header or the current transmission location is not a header when the C (Continue Transmission) command is executed.
X3	ARINC-transmitter (Hardware failure error) - This error will only occur if a failure of the transmitter hardware is detected during the power-up self test or during the T (Test) command execution. If this error is encountered, the channel transmitter will not be available for use. All commands issued to a channel with an ARINC transmitter error will function properly, but the channel will not start data transmission.
X4	Time-base (Hardware failure error) - This error will only occur if a failure of the transmitter Time Base circuits is detected during the power-up self test or during the T (Test) command execution. If this error is encountered, the channel transmitter will not be available for use. All commands issued to a channel with a Time Base error will be accepted and will perform any required I/O functions, but the channel will not start data transmission.
	NOTE: If all four channels have either an ARINC transmitter or Time-base error, the VX4428 transmitter will enter the fatal-error state as listed above.
X5	Channel Transmitting - caused by a command being issued to channel(s) which are currently transmitting when the command requires the channel(s) to not be transmitting.
X6	Delay-time - the frame delay time specified in the header is insufficient for the complete transmission of a frame before the following frame is to begin transmission.
99	There are no errors remaining in the error buffer.

Command: F (Trigger Output)

Syntax: [chan][ftrg][VXItrg]F

Purpose: The F (Trigger Output) command specifies the front-panel and/or VXIbus TTL trigger line to be used as the output trigger line(s) for the specified channel(s).

Description:

[chan] a 1-digit decimal integer from 0 to 4 that specifies the channel(s) affected by the F command. Zero or no parameter specifies all channels.

[ftrg] a 1-digit decimal integer from 1 to 4 that specifies the front-panel trigger line to be used as the trigger output for the channel(s) defined by [chan].

[ftrg]	Trigger line Selected
1	Front-panel transmitter Trigger 0
2	Front-panel transmitter Trigger 1
3	Front-panel transmitter Trigger 2
4	Front-panel transmitter Trigger 3

If any other value other than those listed above are used for the [ftrg] parameter, the front-panel trigger lines will be disconnected from the channel(s) defined by [chan].

[VXItrg] a 1-digit decimal integer from 0 to 7 that specifies the VXIbus TTL trigger line to be used as the trigger output for the channel(s) defined by [chan].

[VXItrg]	Trigger line Selected
0	VXIbus TTL Trigger 0
1	VXIbus TTL Trigger 1
2	VXIbus TTL Trigger 2
3	VXIbus TTL Trigger 3
4	VXIbus TTL Trigger 4
5	VXIbus TTL Trigger 5
6	VXIbus TTL Trigger 6
7	VXIbus TTL Trigger 7

If any other value other than those listed above are used for the [VXItrg] parameter, the VXIbus TTL trigger lines will be disconnected from the channel(s) defined by [chan].

Examples:

1. The command sequence 101F selects the VXIbus trigger line 1 as the output trigger line for channel 1 and disconnects all front panel trigger lines from channel 1.

2. The command sequence 011F (or 11F) selects the front-panel trigger line 0 and VXIbus TTL trigger line 1 as the output trigger lines for all channels.

Errors: A Syntax error will result if an out-of-range value is specified for [chan] or if the number of characters for the [chan], [ftrg], and [VXItrig] parameters exceed 3 characters.

If a Syntax error is generated when the command is received, the command will be ignored.

Command: I (Interrupt Control)

Syntax: [ena]I

Purpose: The I (Interrupt Control) command enables or disables interrupts from the VX4428 transmitter to the System Controller for all channels.

Description: [ena] is a 1-digit decimal integer that specifies the following:

[ena]	Action
0	Interrupts are disabled.
1	Interrupts are enabled.

The VX4428 transmitter interrupts are used to indicate the start of transmission of a frame with the INT bit set in the frame's header word or the completion of an extended header's repeat count. Disabling interrupts with the I command will not affect a currently active VXIbus interrupt or any pending interrupts.

Examples:

1. 0I disables the generation of interrupts to the System Controller.

2. 1I enables the generation of interrupts to the System Controller.

Errors: A Syntax error will result if an out-of-range value is specified for the [ena] parameter.

If a Syntax error is generated when the command is received, the command will be ignored.

Command K (Reset)

Syntax: K

Purpose: The K (Reset) command stops transmitter operation, and returns the VX4428 transmitter to its power-up state.

Description: The K command will immediately stop the ARINC transmitters, regardless of how far the transmissions have progressed or how much data is in each transmitter's FIFO memory. On receipt of the K command, the module is returned to its power-up state with all parameters at the default settings:

Interrupts disabled.
100-kb/s bit rate for all channels.
Transmitter outputs in null state.
Channel 1 is the active channel.
Power LED on.
XMIT1 LED off.
XMIT2 LED off.
XMIT3 LED off.
XMIT4 LED off.
Channel-memory addresses at location 0.
Trigger outputs/inputs for all channels disabled.
Transmitters connected to the auxiliary output connector.

NOTE: This command will not affect any user-loaded data in the message RAM.

Errors: A Syntax error will result if any numerical value immediately precedes the K command.

If a Syntax error is generated when the command is received, the command will be ignored.

Command: L (Load Memory)

Syntax: [len]L

Purpose: The L (Load Memory) command specifies the number of header and/or ARINC data words to be transferred to the active channel's memory.

Description: [len] a 1- to 5-digit decimal integer, from 1 to 32768, that specifies the number of header words and ARINC data words to be sent to the active channel's message RAM.

After the L command is received, all data output to the VX4428 transmitter is treated as binary data and immediately stored in the selected channel's message RAM. Therefore, any <CR> and <LF> characters that might be sent by the system controller after the L command as part of a "normal" output statement must be suppressed; if they are not suppressed, they will be stored in message RAM as part of the channel's message data.

CAUTION:

If an error occurs in the execution of the L command, the command will be aborted and any binary data transferred to the VX4428 transmitter will be interpreted as commands, with unpredictable results.

After completion of the L command data transfer, the current load address of the active channel will be the next address after the address of the last word transferred.

The L command data load can be aborted before the data transfer is completed by issuing a VXIbus Word Serial Clear Command. If the L command is aborted, the current load address will set to the next address following the last complete word loaded.

NOTE: The current load address will be set by the execution of the A, M, or L commands, whichever completed execution last. If the M and L commands are both active when the VXIbus Word Serial Clear command is received, the current load address will be set to the next address following the last complete word loaded with the L command.

Example: 1000L sets the number of header and ARINC data words to be received by the active channel to 1,000 words.

Errors: A Syntax error will result if an out-of-range value is specified for the [len] parameter or if the current load address plus the [len] parameter will exceed 32768.

If an error is generated when the command is received, the command will be ignored.

Command: M (Read Memory)

Syntax: [len]M

Purpose: The M (Read Memory) command prepares the VX4428 transmitter to return the data stored in the active channel's memory.

Description: [len] a 1- to 5-digit decimal integer, from 1 to 32768, that sets the number of 4-byte words to be transferred.

The M command specifies the number of 4-byte words to be read from the active channel's memory starting at the current load address for the active channel.

After completion of the M command data transfer, the current load address of the active channel will be the next address after the address of the last word transferred.

The M command data return will be aborted before the data transfer is completed by issuing a S, E, a new M command, or the VXIbus Word Serial Clear Command. If the M command is aborted, the current load address will set to the next address following the last complete word read.

Following the last 4-byte data word returned to the system controller, terminating <CR> and <LF> characters will be sent to the system controller by the card.

NOTE: The current load address will be set by the execution of the A, M, or L commands, whichever completed execution last. If the M and L commands are both active when the VXIbus Word Serial Clear Command is received, the current load address will be set to the next address following the last complete word loaded with the L command.

Example: 1000M sets the number of header and ARINC data words to be read by the System Controller from the active channel to 1,000 words.

Errors: A Syntax error will result if an out-of-range value is specified for the [len] parameter or if the current load address plus the [len] parameter will exceed 32768.

If an error is generated when the command is received, the command will be ignored.

Command: N (Return ID)

Syntax: N

Purpose: The N (Return ID) command will cause the VX4428 Transmitter to return a string containing the module identification and software version to the system controller on its next request for input from the card.

Description: The string returned by this command is:

CDS VX4428 TRANSMITTER VX.X<CR><LF>

where X.X represents the version of the software.

The N command will be aborted by receiving an M command or the VXIbus word serial Clear command.

Errors: A Syntax error will result if any numerical value immediately precedes the N command.

If a Syntax error is generated when the command is received, the command will be ignored.

Command: O (Relay Open)

Syntax: [chan]O

Purpose: The O (Relay Open) command will open the destination selection relays to connect the transmitters to the VX4428 self-test data path for the specified channel(s).

Description: [chan] a 1-digit decimal integer (or blank) that specifies the channel or channels affected by the O command as follows:

[chan]	Channel(s) Affected
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

NOTE: After the O command has been executed, there will be a 10 millisecond delay to allow the relays to settle before the module will be ready for subsequent commands.

CAUTION:

The relays can be opened (with this command) or closed (with the D command) while the channels are transmitting over the DITS bus. If the relays change position while data transmission is occurring on the DITS bus, transmitted data corruption may occur. It is recommended that the Relay Open command be used only while data transmission is not occurring.

Examples:

1. O or OO will connect all four channels to the self-test data path.

2. 3O will connect channel 3 to the self-test data path.

Errors: A Syntax error will result if an out-of-range value is specified for the [chan] parameter.

If a Syntax error is generated when the command is received, the command will be ignored.

Command: P (Trigger Preset)

Syntax: [chan]P

Purpose: The P (Trigger Preset) command is used to preset the transmitter(s) hardware to start transmission on reception of an external trigger.

Description: [chan] a 1-digit decimal integer that specifies the following:

[chan]	Begin Transmission on Channel(s)
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

The P command has no effect on channels already transmitting or channels preset for external trigger input which are waiting for an external trigger to start transmission.

The P command performs the same functions as the B command except starting transmission on the DITS bus. After the P command is executed, transmission will start when the external trigger input for the channel goes active. The P command can be issued to a channel which has reached the Stop bit in a header with the same qualification on the timing of the command as for the Begin command (the transmitters will be reset for the Begin or Trigger Preset commands).

NOTE: The first frame in memory can not contain an empty frame.

The first frame control bits for each channel will be tested and acted on in the following sequence (assuming that no errors are generated during the command execution):

1. If the Stop bit is set, transmission will not start and the external trigger inputs will not be enabled, but the C command will be enabled for the channel. The P command will continue with the next channel to be pre-set.

2. If the Trigger bit is set, the trigger output will be generated when the first bit is transmitted. (If the first frame is an empty frame, the trigger output will not be generated.) The P command will continue with the next channel to be pre-set.

NOTE: The external trigger input used by the extended header will be reset by the P command prior to arming the channel. The trigger received for the start

of transmission will also cause the first extended header with the external trigger termination enabled to terminate on the first loop.

Examples:

1. 4P pre-sets channel 4.

2. 0P (or simply P) pre-sets all four channels.

Errors:

A Syntax error will result if an out-of-range value is specified for the [chan] parameter.

A Channel Transmitting error will result if the command is issued to a channel currently transmitting or waiting for an external trigger to start transmission.

A Frame-header Missing error will result if the command is issued to a channel which does not have a header loaded into the first location in memory.

If a Syntax error is generated when the command is received, the command will be ignored. If a Channel Transmitting or Frame-header Missing error is generated, the channel which encountered the error will not be pre-set.

Command: Q (Quit Transmission)

Syntax: [chan]Q

Purpose: The Q (Quit Transmission) command stops transmission for the specified channel(s).

Description: The Q command stops transmission at the end of the last word sent to the transmitters. Transmission may stop at any point within a frame, including the last word in the frame. To ensure that transmission stops at the end of a frame, the Stop bit in the header should be used instead of the Q (Quit Transmission) command.

[chan] a 1-digit decimal integer that specifies the following:

[chan]	Channel(s) Affected
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

Within the VX4428 transmitter, data for each channel is moved from main memory in blocks of eight ARINC words, to a separate, 16-ARINC-word, high-speed, FIFO memory which drives a given channel's DITS data bus. When a Q command is issued, the specified channel will not stop transmission until the FIFO memory associated with the channel has emptied. If a Q command is to be followed by a B command to restart transmission from the first word in memory, a time delay equal to 576 times the programmed bit rate should be placed between the Q and B commands. Failure to do so may result in data transmission stopping in the middle of an ARINC word.

Examples:

1. 0Q or Q stops transmission on all four channels.

2. 2Q stops transmission on channel 2.

Errors: A Syntax error will result if an out-of-range value is specified for the [chan] parameter.

If a Syntax error is generated when the command is received, the command will be ignored.

Command: R (Bit Rate)

Syntax: [per]R

Purpose: The R (Bit Rate) command specifies the period (in nanoseconds) of the bit-rate clock for the active channel.

Description: [per] a 2- to 5-digit decimal integer, from 32 to 32767, that sets the bit-rate clock based on the following equation:

bit-rate frequency (Hz) = 1 / ([per] . 10^{-9} . 250)

Examples:

1. 32R specifies a bit-rate frequency of 125 kHz (125 kb/s) for the active channel.

2. 40R specifies a bit-rate frequency of 100 kHz (100 kb/s) for the active channel.

3. 320R specifies a bit-rate frequency of 12.5 kHz (12.5kb/s) for the active channel.

Errors: A Syntax error will result if an out-of-range value is specified for the [per] parameter.

A Channel Transmitting error will result if the command is issued to a channel currently transmitting.

If a Syntax or Channel Transmitting error is generated when the command is received, the command will be ignored.

Command: S (Select Active Channel)

Syntax: [chan]S

Purpose: The S (Select Active Channel) command selects the active channel for subsequent commands.

Description: [chan] a 1-digit decimal integer from 1 to 4 that specifies the active channel as follows:

The S command will set the current transmission address return to the new channel upon execution. Any characters remaining from the previous channel will be lost. The S command will only affect operations if the new channel is different from the old channel.

Example: 3S selects channel 3 as the active channel for future commands from the system controller.

Errors: A Syntax error will result if an out-of-range value is specified for [chan].

If a Syntax error is generated when the command is received, the command will be ignored.

Command: T (Self Test)

Syntax: T

Purpose: The T (Self Test) command performs a functional self test of the VX4428 transmitter.

Description: During the functional self test, the message RAM is fully tested, the output transmitters are looped back to a processor input port and checked prior to the final differential drive amplifiers, and the channel counter/timers and interrupt controllers are tested. After this test is performed, all data stored in message RAM is lost, and the card returns to its power-up state (see the Specification section for a full description of the power-up state). The error code for any errors found during self test can be read back using the E (Error Return) command. This test takes approximately 28 seconds to perform.

Any characters received by the VX4428 transmitter following the T command will not be processed until the functional self test is complete. To avoid appearing to "hang up" the system controller during the self test period, any terminating <CR> or <LF> characters "normally" output by the system controller following the T command should be suppressed.

Errors: A Syntax error will result if any numerical value immediately precedes the T command.

If a Syntax error is generated when the command is received, the command will be ignored.

Command: V (Voltage Level)

Syntax: [sel][lev]V

Purpose: The V (Voltage Level) command specifies the transmission voltage level for the active channel's transmitter.

Description: [sel] a 1-digit decimal integer from 0 to 4 that specifies the following:

[sel]	Voltage level selected
0, or no parameter	Normal ARINC-429
1	Parametric high
2	Parametric low
3	Parametric null
4	Direct voltage level selection using the [lev] parameter.

[lev] a 1 to 3-digit decimal integer from 0 to 255 that specifies the transmission voltage level using the following formula:

Voltage level = [lev] * (volts/step)
(See the Specifications section for the volts/step value).

This parameter is required when the value of [sel] is '4'. If the parameter is included for those values of [sel] in which it is not required, the parameter will be ignored.

The Normal ARINC-429 data levels and parametric high, low, and null data levels are defined in the SYSFAIL, Self Test and Initialization section of this manual.

Errors: A Syntax error will result if an out-of-range value is specified for the [sel] or [lev] parameters.

A Command Transmitting error will be generated if the active channel is transmitting when the command is received.

If a Syntax error is generated when the command is received, the command will be ignored.

Command: X (Trigger Input)

Syntax: [chan][trgln]X

Purpose: The X (Trigger Input) command specifies the front-panel or VXIbus TTL trigger line to be used as the external trigger for the specified channel(s).

Description: [chan] a 1-digit decimal integer from 0 to 4 that specifies the channel(s) affected by the X command.

[trgln] a 2-digit decimal integer that specifies the front-panel or VXIbus TTL trigger line to be used as the external trigger for the channel(s) defined by [chan]:

[trgln]	Trigger line Selected
00	VXIbus TTL Trigger 0
01	VXIbus TTL Trigger 1
02	VXIbus TTL Trigger 2
03	VXIbus TTL Trigger 3
04	VXIbus TTL Trigger 4
05	VXIbus TTL Trigger 5
06	VXIbus TTL Trigger 6
07	VXIbus TTL Trigger 7
08	Front-panel Trigger 0
09	Front-panel Trigger 1
10	Front-panel Trigger 2
11	Front-panel Trigger 3

If any values other than those listed above are used for the [trgln] parameter, the front-panel and VXIbus TTL trigger lines will be disconnected from the channel(s) defined by [chan].

CAUTION: Changing the external trigger line for a channel which has already been preset could result in false triggering.

Examples:

1. The command sequence 101X selects the VXIbus trigger line 1 as the external trigger for channel 1.

2. The command sequence 011X (or 11X) selects the front-panel trigger line 4 as the external trigger for all channels.

Errors: A Syntax error will result if an out-of-range value is specified for [chan] or if the number of characters for both the [chan] and [trgln] parameters is more than 3 characters.

If a Syntax error is generated when the command is received, the command will be ignored.

Receiver Operation

The receiver tests and analyzes data received from the Mark 33 Digital Information Transfer System (DITS) found on many commercial aircraft. The VX4428 receiver has four independent receivers, each with an associated buffer memory for storing up to 32,000 ARINC-429 words (four bytes each) received on the DITS bus, for a total of 512,000 bytes of on-card memory. Programmable data capture modes offer great flexibility in testing and analysis.

The VX4428 receiver captures ARINC-429 data using one of the following four primary data-capture Activity modes. Each of the four channels is separately programmable.

- Monitor Mode

  In Monitor Mode, the VX4428 receiver captures all ARINC-429 traffic received on the DITS bus and sequentially stores the captured data in the card's memory.

- Select-labels Monitor Mode

  In Select-labels Monitor Mode, the VX4428 receiver stores data based on a user-defined list of up to six ARINC-429 labels for each of four channels. For each of the six user-defined labels, the Select-labels Monitor Mode also allows the data to be captured to be further restricted by defining the value of the source/destination-identifier (SDI) field and/or the sign/status-matrix (SSM) field. (Use of the SDI and SSM fields is defined in the ARINC-429 Specification.)

- Limit-check Mode

  In Limit-check Mode, the VX4428 receiver will store ARINC-429 data based on a data limit condition for a single user-defined label, optionally qualified with the SDI and/or SSM field values. The module will automatically disable data reception after the data limit condition is met and the pre-defined number of data words following are stored.

- All-label Mode

  In All-label Mode, the VX4428 receiver allocates one specific location in memory for all 256 possible ARINC-429 labels, optionally qualified with the SDI and/or SSM field value. The module will store only the latest data received for each label.

In each of the primary data-capture modes, the VX4428 receiver allows data to be stored in one of the following three ways:

- ARINC-429 data words only.

- ARINC-429 data words plus time-stamp and error bytes.

- Only those ARINC-429 data words (including time-stamp and error bytes) in which an error has occurred.

Data stored in memory can be read while the VX4428 receiver is receiving data with no loss of data. In Monitor and Select-label modes, the data is stored in a first-in-first-out (FIFO) structure. This means that reading data effectively frees up those storage locations for further data capture. In All-labels mode, memory is continuously updated to reflect the most current data. Older data is not retained by the module. In Limit-check mode, the most current data received is available to the system controller until the trigger event occurs. At that point, the number of words previously specified is stored and retained until the receiver is re-enabled, the mode for that channel is changed, or the data storage method is re-specified.

The Limit-check and Monitor Mode trigger events are also available as one or more of four front panel trigger outputs, or may be connected to multiple selected VXIbus backplane TTLTRG lines.

The independent time-stamp counters on each receiver channel of the VX4428 receiver are reset when the receiver is enabled. This provides an indication of the exact time when an ARINC-429 word was received (with respect to start of data collection), for any channel. The default setting for the programmable 16-bit counters is 1 ms, but they can be programmed from a 10 microsecond resolution up to 109 minutes before re-starting at zero again.

The VX4428 receiver provides isolation relays which allow the receiver and transmitter to be connected for a full wrap-around self test.

This section contains the following subsections:

- Overview of each of the four primary Activity modes.
- Description of the data format for capture labels and secondary capture definition (SSM, SDI), and the data format for returned ARINC-429 label/data information, error and time-stamp values. These formats are referred to in the detailed command descriptions.
- Description of methods of data capture for each Activity Mode. For example, single data word, blocked data formats for all words collected or for a specified number of data words are provided, depending on the Activity mode.
- Interrupt generation.
- Trigger Output generation.
- Descriptions of each of the module commands. A summary lists the global and active channel commands in alphabetical order. This is followed by a detailed description of each command, including examples and errors.

Activity Modes

Monitor Mode

In this mode, the VX4428 receiver captures all data traffic on the ARINC-429 bus and stores the data sequentially in the card's memory. In Monitor Mode, data storage is organized as a first-in/first-out (FIFO) memory.

If the FIFO memory becomes full, any new data to be stored will be lost and an error will be generated. To prevent this overflow condition from occurring, the VX4428 receiver can generate an interrupt to the system controller when the FIFO memory becomes ¾ full. This gives time to read data from memory, thus making room for new data.

The Monitor Mode can also generate a trigger output based on a user-supplied list of up to six message masks. Each mask consists of one to four bytes corresponding to each of the four bytes contained in an ARINC word.

Select-labels Monitor Mode

In this mode, the VX4428 receiver captures data based on a user-defined list of up to six ARINC-429 labels for each of four channels (up to 24 different labels may be defined if all four channels are connected to the same bus), and stores the data sequentially in the card's memory. Labels are defined by outputting a list of labels and secondary-mode bytes to the VX4428 receiver. (See the LC and LL commands in the Module Commands subsection for details on how to load labels and secondary-mode bytes.) The proper formats for the label and secondary-mode bytes are shown in the Label Byte Format and Secondary Mode Byte Format sub-sections.

As in the Monitor Mode, data storage is organized as a FIFO memory with an error generated for memory overflow and a ¾ memory interrupt capability.

Limit-check Mode

In Limit-check Mode, the VX4428 receiver captures data for a single user-defined ARINC-429 label. The label is defined by outputting a label and secondary-mode byte to the module (see the SL command). The proper formats for the label and secondary-mode bytes are shown in the Label Byte Format and Secondary Mode Byte Format subsections.

The VX4428 receiver checks the data for the defined label against a user-defined limit (see the LP command). A 'greater than', 'equal to', or 'less than' 23-bit binary comparison will be made between the user-defined limit and the received data. The trigger event is defined as the received data which meets the specified comparison.

In the Limit-check Mode, data is stored based upon the trigger event and a user-defined pre-trigger and post-trigger number of words.

Once the trigger event has occurred and the pre-set number of words after the trigger event have been received, the receiver will be disabled and the data block defined by the pre-trigger and post-trigger number of words will be available for readback. The size of the data block available for readback is equal to a) the total of the pre-trigger value, post-trigger value, and one word for the trigger event, or b) the number of words received, whichever is less.

The Limit-check Mode can also generate an interrupt and/or a trigger output upon completion of data storage.

All-label Mode

In this mode, the VX4428 receiver captures and stores all ARINC-429 data received. Each ARINC-429 label or the label and the SDI and/or the SSM fields has one specific RAM location that is accessible by sending the label and secondary-mode bytes to the module (see the BT command). Only the latest data for each label or label/SDI/SSM combination is saved.

Formats

Loading Labels and Secondary Mode Bytes

The following formats are used with the LC, LL, and SL commands to specify the labels to store for the Select-labels Monitor Mode and Limit-check Mode, and with the BT command to specify the labels to return data for in the All-label Mode.

The label and secondary-mode bytes for the Select-labels Monitor Mode, Limit-check Mode, and the All-label Modes are loaded sequentially into the VX4428 receiver's memory as label/mode-byte pairs. The label/mode-byte pairs are output to the VX4428 receiver in the following sequence:

ARINC-429 label 1
Secondary-mode byte 1
.
.
.
ARINC-429 label n - 1
Secondary-mode byte n - 1
ARINC-429 label n
Secondary-mode byte n

In the Select-labels Monitor Mode the variable "n" has a maximum value of 6, with each pair individually addressable (see the LC and LL commands in the Command section of this manual).

In the Limit-check Mode, only a single pair is loaded. (See the SL command in the Command section of this manual).

In the All-label Modes the variable "n" has a maximum value of 50. (See the BT command in the Command section of this manual).

Label Byte Format

The label field used in commands for the Select-labels Monitor Mode, Limit-check Mode, and the All-label Modes is a single character in 8-bit binary format:

Label byte:

Bit Position	7	6	5	4	3	2	1	0
ARINC-429 Bit Position	1	2	3	4	5	6	7	8

Secondary Mode Byte Format

The secondary-mode byte field used in the commands for the Select-labels Monitor Mode, Limit-check Mode, and the All-label Modes is a single character in 8-bit binary format:

Secondary mode byte:

Bit Position	7	6	5	4	3	2	1	0
ARINC-429 Bit Position					10	9	31	30
Data	SDI	SSM			SDI2	SDI1	SSM2	SSM1

SDI and SSM Bits

The SDI and SSM bits are mode selection bits that enable the secondary capture modes used in Select-labels Monitor Mode and the Limit-check Mode. In the All-label Modes the SDI and SSM mode selection bits are ignored. (SDI and SSM mode selection are as defined by the selected All-labels sub-mode.)

Table 5 lists the values of the SDI and SSM bits which define the different secondary capture modes.

TABLE 5: Secondary Capture Modes

SDI	SSM	Mode
0	0	Capture data based on label only.
0	1	Capture data based on label and SSM.
1	0	Capture data based on label and SDI.
1	1	Capture data based on label, SDI, and SSM.

SSM1 and SSM2 Bits

The SSM1 and SSM2 bits define the value of the SSM field for the label to be captured in the Select-Labels Monitor Mode and the Limit-Check Mode. In the All-label Mode, SSM1 and SSM2 define the value of the SSM field for a label's data to be returned if data storage is being qualified by the SSM field (see MM command modes 5 and 6), otherwise SSM1 and SSSM2 are ignored.

SDI1 and SDI2 Bits

The SDI1 and SDI2 bits define the value of the SDI field for the label to be captured in the Select-Labels Monitor Mode and the Limit-Check Mode. In the All-label Mode, SDI1 and SDI2 define the value of the SDI field for a label's data to be returned if data storage is being qualified by the SDI field (see MM command modes 4 and 6), otherwise SDI1 and SDI2 are ignored.

Limit Byte Format

In the Limit-check Mode it is necessary to load limit bytes as a standard of comparison for incoming data by using the LP command. The limit bytes consist of three characters in 8-bit binary format:

Limit bytes:

Bit Position	7	6	5	4	3	2	1	0
	ARINC-429 Bit Position							
Byte 1	16	15	14	13	12	11	10	9
Byte 2	24	23	22	21	20	19	18	17
Byte 3	N/U	31	30	29	28	27	26	25

Bit position 32 of the ARINC-429 word is not used for limit checking. If the SDI field is used for the label-selection process, ARINC-429 bits 9 and 10 are not used for limit checking. If the SSM field is used for the label-selection process, ARINC-429 bits 30 and 31 are not used for limit checking. The comparison assumes that both the limit value and the value to be compared are unsigned, positive magnitude integers.

Label/Data Read Format

ARINC-429 defines bit ordering differently for the label and the data. For the label, the first bit transmitted on the ARINC-429 bus is the most significant bit. For the data, the first data bit transmitted on the bus is the least significant bit.

If the label and data were both stored in transmitted order, the system controller would have to perform a bit reversal on the label. To eliminate this system controller requirement, the VX4428 receiver reverses the label bit order in hardware, which allows the system controller to use the label and data bytes without having to reverse bit position.

In all four primary data-capture modes, data is read back from a channel of the VX4428 receiver using one of the following two formats based on the data storage mode selected.

o Four bytes are returned when only ARINC-429 data words are stored.

4-byte format (ARINC-429 data only):

Bit Position	7	6	5	4	3	2	1	0
	ARINC-429 Bit Position							
Byte 1	1	2	3	4	5	6	7	8
Byte 2	16	15	14	13	12	11	10	9
Byte 3	24	23	22	21	20	19	18	17
Byte 4	32	31	30	29	28	27	26	25

Byte 1 is the label. Byte 2 is the least significant data byte. Byte 4 is the most significant data byte.

o Eight bytes are returned when time-stamp and error bytes are stored along with the data.

8-byte format (ARINC-429 data with time-stamp and error bytes):

Bit Position	7	6	5	4	3	2	1	0
	ARINC-429 Bit Position							
Byte 1	1	2	3	4	5	6	7	8
Byte 2	16	15	14	13	12	11	10	9
Byte 3	24	23	22	21	20	19	18	17
Byte 4	32	31	30	29	28	27	26	25
Byte 5	Error byte							
Byte 6	Reserved							
Byte 7	Time-stamp byte 2							
Byte 8	Time-stamp byte 1							

Error Byte

Data errors are returned in byte 5 of the 8-byte format whenever storage of data with time-stamp and error bytes is selected. The format of the error byte is as follows:

Bit Position	7	6	5	4	3	2	1	0
Byte 5	0	0	0	0	IWG	LSE	0	PE

The error bits have the following meanings when set high:

IWG Interword-gap time < nominal (35 µs for 100-kb/s; 266 µs for 12 to 14.5 kb/s data rate).

LSE Number of bits received for ARINC-429 word < 32 bits.

PE Parity for received ARINC-429 word is not odd.

33-Bit Errors

33-bit words received at the slow bit rate will be indicated by the correct storage of the first 32 bits stored as one word, followed by a word with all bits set to zero and, if time stamp error bytes are stored, an IWG (InterWord Gap time) error and LSE (number of bits received) error indicated. 33-bit words received at the fast bit rate will be stored

the same as at the slow bit rate, with the addition that if another word follows the first within the minimum IWG time, the following (second) word will be stored incorrectly.

Time-Stamp Bytes

Time-stamp bytes are the last two of eight bytes that appear when reading back data with time-stamp and error bytes. The time-stamp bytes reflect the current state of a 16-bit counter which is set to zero when a channel's receiver is enabled or when the counter overflows. Independent counters are provided for the four channels. The format of the two time-stamp bytes is as follows:

Time-stamp bytes:

Bit Position	7	6	5	4	3	2	1	0
Byte 7	T15	T14	T13	T12	T11	T10	T9	T8
Byte 8	T7	T6	T5	T4	T3	T2	T1	T0

Table 6 lists the decimal value associated with each bit in the two time-stamp bytes. If one or more bits are set high, the respective values are summed; the resultant is then multiplied by the time-stamp resolution (see TR Command) to produce the time-stamp value. In other words, the two time-stamp bytes simply contain a 16-bit binary number which is multiplied by the time-stamp resolution to produce the time-stamp value.

TABLE 6: Time-stamp Value
(N x Time-stamp Resolution)

Bit	N
T0	1
T1	2
T2	4
T3	8
T4	16
T5	32
T6	64
T7	128
T8	256
T9	512
T10	1,024
T11	2,048
T12	4,096
T13	8,192
T14	16,384
T15	32,768

Example:
Assume the time-stamp resolution is set to 1 ms. If byte 7 is equal to A7h (T15, T13, T10, T9, and T8 set high), and byte 8 is equal to 51h (T6, T4, and T0 set high), then the sum of all the high bits is 42,833. Multiplying this times the time-stamp resolution indicates 42.833 seconds since the receiver was enabled or since the counter last overflowed. [The decimal value 42,833 may also be determined by multiplying the decimal value of byte 7 (167) by 256 and adding the decimal value of byte 8 (81).]

NOTE: When time-stamp and error bytes are stored with ARINC-429 data words, the maximum number of ARINC-429 words stored for the Monitor, Select Labels Monitor, and Limit-check Mode of each channel is reduced by half. For example, the memory capacity in Monitor Mode, normally 32,000 words per channel, becomes 16,000 words per channel when time-stamp and error bytes are stored.

Data Access

Modes

In Monitor Mode and Select-labels Monitor Mode, ARINC-429 data words and time-stamp bytes can be accessed in three ways:

1. The next data word in the FIFO memory is returned in response to an input request. This is the default data-access method in effect at power-up, and upon

completion of the other two data-access methods. If an input is requested and no new data is available, a 'pad' word (all bits = 1) is returned.

2. A specified number of data words are returned in response to an input request. If the number of words specified exceeds the number of data words currently stored, then the module will return to the first data-access method once the data words currently stored have been returned.

3. All data words stored in the FIFO memory are returned in response to an input request. In this data-access method, two bytes are prefixed to the returned data. These two bytes contain the binary value for the number of ARINC-429 words stored at the time of the input request. The first byte returned is the low-order byte; the second byte returned is the high-order byte. Following these two bytes, data is returned beginning with the first word stored in memory. After returning all data words stored in memory, the VX4428 receiver returns to the first data-access method.

In Limit-check Mode, ARINC-429 data words and time-stamp bytes can be accessed in two ways:

1. While the channel is storing data, one data word is returned, which is the most current at the time the input request is received.

2. After the trigger event has occurred and the post-trigger number of words have been captured, then the three data access methods listed for the Monitor Mode can be used. All data reads for the Limit-check Mode are nondestructive reads. Once the last word stored has been read, data reads will start over with the first word stored in memory.

In All-Label Modes, the most current ARINC-429 data words and time-stamp bytes for the defined list of labels (see the BT command) are returned in response to an input request.

Termination Characters

Both of the block transfer modes for Monitor, Select-Labels and Limit-Check modes described above return a <CR><LF> after the required number of words have been transferred. The Monitor and Select-labels single word transfer modes will continue to return data without a <CR><LF> terminator as long as additional data is available. A terminating <CR><LF> will be sent when no more data is available. If additional input requests are made with no data available, a pad byte followed by a <CR><LF> will be returned. A pad byte followed by a <CR><LF> will also be returned on an initial input request if no data is yet available.

The Limit-check Mode will never send a <CR><LF> in the single word mode; the latest data will always be sent while still receiving data. Or, if collection is complete, the pre- and post-trigger memory is treated as an unending circular buffer with no termination.

The All-labels mode is terminated with a <CR><LF> following the return of all data specified by the All-label mode label list.

The data-access method can be changed before the previous method has been completed without causing any data to be lost. Also, other commands may be sent to the VX4428 receiver while it is accessing data with any of the described methods, without causing any data to be lost.

Termination of Input with the System Controller

System controllers typically allow reading data by one or more of the following four methods:

A One byte is read at a time. This method is usually used when reading non-printable characters (in applications where the data returned uses the full eight bits for data content, rather than limiting return alphanumeric and associated printable characters). This mode is usually called a 'binary read'.

B Read a specified number of bytes. This method is also used for non-printable characters. It is sometimes called a 'binary block read' or a 'block read'.

C Read until a specified terminator character (usually a line-feed) is received. This method is often used for reading ASCII text strings.

D Read until an end-of-transfer indication is received. In IEEE-488 systems, this is provided by the EOI (End Or Identify) signal. In embedded controllers specifically designed for the VXIbus, this signal may be provided by drivers that recognize the VXIbus End bit (bit 8 of the Data Low Read VXIbus Communication register; bits 7-0 contain the data).

Method C is not recommended for use with the VX4428 receiver when reading ARINC-429 data, since reads may be terminated prematurely in the middle of an ARINC-429 32-bit word or in the middle of a time-stamp value if the 8-bit code for a byte happens to be the same as a line feed code. This problem may be application-dependent, and not show up during application software development, and is often hard to troubleshoot because of random occurrence.

Method D can be a useful way to read data from the VX4428 receiver in all modes except the Limit-check mode. The VX4428 receiver is designed to set the VXIbus End bit when a <LF> terminator character is returned, but not if the data content is equivalent to a line feed code. All of the VX4428 receiver modes except the Limit-check mode send a <LF> terminator character when no more data is available. This method eliminates the need to look for pad bytes, except as the first byte, to indicate no data is available.

The drawbacks to method D are that a non-IEEE-488 or non-VXIbus designed controller won't support it, the reading rate of the controller may not be as fast as the ARINC-429 data transfer rate (in which case the read will not terminate), or the string length or

buffer size available for the read operation may be smaller than the amount of data available.

Method B is the safest way to read data from the VX4428 receiver, and with the two block-data transfer modes provided, also gives excellent transfer rate performance.

One of the block transfer methods allows specifying the number of words to be read. The buffer size for the read may then be calculated by multiplying the word count by 4 or 8 (depending on whether time-stamp is specified) and adding 2 for the terminator character.

The second block transfer mode returns the word count as the first two bytes. This word count may be used to calculate the remaining byte count as just described for the other block transfer mode. In the All-labels mode the byte count may be determined in a similar manner from the number of labels specified by the BT command.

For those who don't wish to deal with the terminator character, the VX4428 receiver may be programmed to suppress the terminator character with the TD command.

Method A should only be used if method B is not supported in the system controller or by the programming language used. If this method must be used, a VX4428 receiver block transfer data access method is still recommended for easier tracking of byte count. Method A will require use of loop counters in the application program and will not provide the transfer rate performance of method B.

Interrupt Generation

When enabled, the interrupt generation capability of the VX4428 receiver will generate a VXIbus request true interrupt to its interrupt handler (usually its commander) depending on one of the following two conditions:

1. In Monitor Mode or Select-labels Monitor Mode, interrupts are generated when the memory becomes 3/4 full. This interrupt is provided to prevent new data from being lost when the memory becomes completely full.

2. In Limit-check Mode, interrupts are generated when the trigger event has occurred and the preset number of bytes have been stored (see the PT and PR commands).

If the module encounters a new interrupt condition after an interrupt has been generated, a new interrupt will be generated after the initial interrupt has been acknowledged. In order for a new interrupt to be generated, the present interrupt must be acknowledged by both a VXIbus interrupt acknowledge cycle and a VXIbus word serial Read STB command.

The Read STB command will return an 8-bit byte of data in the following format, after the VXIbus interrupt acknowledge cycle has occurred:

Read STB Response

Bit Position	7	6	5	4	3	2	1	0
	0	1	1	1	chan 4	chan 3	chan 2	chan 1

A value of 1 in bits 3-0 indicates which channel(s) is generating the interrupt.

In an IEEE-488 controlled system, the VX4428's interrupt handler, commander, and the IEEE-488-to-VXIbus interface will typically be on the same VXIbus module. This module will typically generate an IEEE-488 Service Request (SRQ) in response to the VXIbus Request True interrupt. A serial poll from the controller will then cause the Read STB to be issued to the VX4428, and the byte returned by the VX4428 receiver will be returned as the serial poll byte value.

The EX command may be used when VXIbus interrupts are disabled, to monitor the channels for conditions which would normally cause an interrupt. This also requires that the module interrupts have been disabled with the IN command.

Trigger Output Generation

When enabled, the trigger output generation capability of the VX4428 receiver will generate a VXIbus backplane TTLTRG trigger and/or a Front-panel trigger output in the Limit-check Mode when the trigger event has occurred and the preset number of bytes have been stored (see the PT an PR commands).

System Commands

Although these non-data commands are initiated by the VX4428's commander rather than the system controller, they have an effect on the VX4428 Module. Refer to the commander's Operating Manual for information on the VXIbus Instrument Protocol Commands that will affect the VX4428.

Module Commands

A summary of the VX4428's receiver commands is listed below, and a description of the required order of programming needed for commands. This is followed by detailed descriptions of each of the commands. A sample program using these commands is shown in Section 4.

Command Syntax

Command protocol and syntax for the VX4428 receiver are as follows:

1) If a character is not enclosed by brackets, that character itself is sent, otherwise:
   [ ] encloses the symbol for the actual argument to be sent. These argument symbols are defined under each command heading.

<CR> indicates a carriage return.
<LF> indicates a line feed.

2) Any character may be sent in either upper or lower case form.

3) Any of the following white space characters:
   00 hex through 2F hex
   3A hex through 40 hex
   5B hex through 60 hex
   7B hex through FF hex
are allowed at any time as spacers, except when binary data is being transferred. Note that both <CR> and <LF> are included as white space characters. This means that they are neither required nor prohibited as terminators for commands sent to this module.

4) When binary data is referenced as a command parameter it is intended to be sent as an 8-bit binary value.

   For example, the numeric character '3' is represented in 8 bit ASCII as "00110011" with each zero (0) or one (1) representing a single bit from high bit position to low bit position. In straight 8-bit binary the value of '3' is represented as "00000011". When a binary value is required it is the second format which must be used.

5) Any character not explicitly defined as binary is to be sent in ASCII.

Summary

Detailed descriptions of each command (in alphabetical order) are given following the summary. The command summary is divided into two sections: Global commands and Active Channel commands. A description of the required order for programming follows.

Global Commands Summary

Global commands function independently of the active channel.

Command Action

CD Clear Data - Clears the channel(s) message RAM.

CL Clear Label - Clears the channel(s) stored capture label(s) for the Select-labels Monitor or Limit-check Modes.

ER Error Return - Sets the VX4428 receiver to return the error codes for all programming or hardware errors stored.

EX Examine Status - Sets the VX4428 receiver to return the Module's status byte.

ID Return ID - Returns a string containing the module identification and software version to the system controller on its next request for input from the card.

RC Relay Close - Closes the source selection relay(s) to connect the receiver(s) to the input connector.

RD Receiver Disable - Disables data reception for a single channel or for all four channels.

RE Receiver Enable - Enables data reception for a single channel or for all four channels.

RO Relay Open - Opens the source selection relay(s) to connect the receiver(s) to the VX4428 self-test data path.

RS Reset - Stops the receiver operation and returns the VX4428 receiver to its power-up state.

SC Select Channel - Selects the channel to be active for subsequent channel commands.

ST Self Test - Used to perform a complete self test of the VX4428 receiver.

TE Trigger Output Enable - Defines whether the front panel and/or the backplane trigger output lines will be enabled/disabled.

TR Time-stamp Resolution - Sets the time-stamp resolution value for all four channels.

TS Trigger Line Select - Defines which of the trigger output lines for the front panel and the backplane trigger output lines will be used.

Active Channel Commands Summary

These channel-specific commands affect only the active channel.

Command Action

BR Bit Rate - Selects a slow (12 to 14.5 Kb/s) or a fast (100 Kb/s) bit rate for the received data.

BT Block Transfer - Defines the list of labels whose data will be returned for the All-label Modes.

DS Data Storage - Sets the type of data words to be stored.

IN Interrupt - Enables or disables module interrupts.

LC Label Change - Selectively changes one label in the list of capture labels for the Select-label Monitor Mode.

LL Load Labels - Specifies a set of labels and secondary capture modes for the Select-labels Monitor Mode.

LM Load Monitor Labels - Specifies a set of data words to be used by the Monitor Mode to generate trigger outputs for the active channel.

LP Limit Parameters - Sets the value of the limit parameter and the type of comparison for the Limit-check Mode.

MM Main Mode - Selects one of the four primary capture modes (Monitor, Select-labels, Limit-check, and All-labels), and selects one of four sub-modes in the All-labels mode.

PR Pre-Trigger - Sets the number of words to store before the trigger event has occurred for the Limit-check Mode.

PT Post Trigger - Sets the number of words to store after the trigger event has occurred for the Limit-check Mode.

SD Select Data - Specifies the data word return format as a single word or as one of the two block transfer modes for Monitor and Select-labels modes.

SL Set Label - Defines the capture label and secondary mode byte for the Limit-check mode.

TD Terminate Data - Defines whether or not <CR><LF> is appended to the end of a response data transfer.

Command Order

The order in which commands are programmed is significant, and depends on the mode being used. If required commands are not present, or are not in the correct sequence, errors may result. The usual order of commands is as follows:

RS (Reset) - When this command is issued, it resets the VX4428 receiver to its power-up state. All receivers are disabled, the RAMs are cleared, any data label lists are cleared, and default activity modes and time-stamp resolution are selected. The VXIbus interface is unaffected.

RC (Relay Close) - This command is issued to connect the receivers to the input connector.

TR (Time-stamp Resolution) - This command may be issued first to set the time-stamp resolutions for all four channels. This command is not necessary if time-stamping of the data is not required.

SC (Select channel) - The individual channels may now be selected, and the mode, capture label, bit rate, data capture and data readback, etc. specified for each channel.

The BR (Bit Rate), MM (Main Mode), and DS (Data Storage) commands select fast or slow bit rate, the activity mode, and whether error and time-stamp information are to be stored with the data. A TD (Terminate Data) command may be sent to specify termination of data transfers with a <CR><LF>. An IN (Interrupt) command may be sent to enable interrupts. These commands may be sent in any order.

If the Monitor Mode has been selected, the channel is now ready for operation and the receiver may be enabled with the RE (Receiver Enable) command for data collection.

If the Select-label Mode has been programmed, an LL (Load Labels) command may be issued to define up to six capture labels, optionally including SDI and SSM capture specifications. An LC (Label Change) or CL (Clear Labels) command may be used to selectively change one of the six capture labels, or to clear the capture label list for redefinition. The Select-label Monitor Mode is now ready for operation and the receiver may be enabled with the RE (Receiver Enable) command for data collection.
If the Limit-check Mode has been programmed, an SL (Set Label) command and an LP (Limit Parameters) command are sent to define the single capture label with optional SDI and SSM bit capture specification and the limit-check trigger word. A PR (Pre-trigger) and/or PT (Post-trigger) command may optionally be sent to specify the number of words collected prior to the limit-check trigger event and the number of words to be collected after the trigger event.

The Limit-check Mode is now ready for operation and the receiver may be enabled with the RE (Receiver Enable) command for data collection.

The All-label Mode has four sub-modes, previously defined by the MM (Main Mode) command. Depending on the sub-mode selected, either 256, 1024, or 4096 separate 'mailboxes' are set up with the latest data for each label/SDI/SSM combination stored in each.

In the All-label Mode, a BT (Block Transfer) command is sent to define a list of labels (optionally including secondary mode SDI/SSM specifications) to be sent as a block of data. A CD (Clear Data) command is required to clear old data stored for all labels to ensure that only new data is present after the receiver is enabled.

The All-label Mode is now ready for operation and the receiver may be enabled with the RE (Receiver Enable) command for data collection.

The next channel may now be selected and programmed. All channels may be set up and the receiver enabled at the same time with the RE (Receiver Enable) command, if desired. The receiver may be disabled with the RD (Receiver Disable) command and data then collected in the format specified, or data may be read "on-the-fly" while the receivers are enabled.

The following summary outlines the commands typically sent for each of the four primary activity modes of the VX4428 receiver:

For all modes:
RS (Reset)
RC (Relay Close)
TR (Time-stamp Resolution)
SC (Select Channel)
BR (Bit Rate)
DS (Data Storage)
TD (Terminate Data)
IN (Interrupt)
MM (Main Mode)
ID (Return ID)

For Monitor Mode:
SD (Select Data)
TS (Trigger Select)
TE (Trigger Enable)
RE (Receiver Enable)
LM (Load Masks)

For Select-label Mode:
SD (Select Data)
LL (Load Label)
CL (Clear Label)
LC (Label Change)
TS (Trigger Select)
TE (Trigger Enable)
RE (Receiver Enable)

For Limit-check Mode:
SL (Set Label)
LP (Limit Parameters)
PR (Pre-trigger)
PT (Post-trigger)
TS (Trigger Select)
TE (Trigger Enable)
RE (Receiver Enable)

For All-label Mode:
BT (Block Transfer)
CD (Clear Data)
RE (Receiver Enable)

The following list shows which of the above commands are required, and which are optional.

Required	Optional
Start-up:	
RC	RS
	TR
All channels:	
BR	DS
MM	IN
SC	TD
	ID
Monitor Mode:	
RE	SD
	TE
	TS
	LM

Required	Optional
Select-label Mode:	
LL	CL
RE	LC
	SD
	TE
	TS
Limit-check Mode:	
LP	PR
RE	PT
SL	TE
	TS
All-label Mode:	
BT	
CD	
RE	

Except for the BT, IN, SD, and TD commands, all channel-specific commands must be sent while the receiver is disabled. Of the global commands, the TR and CL commands must also be sent while the receiver is disabled.

The command order listed above is provided as a guide for first-time programmers of the VX4428 receiver. Command ordering may be changed as long as the following rules are observed:

1. Commands that are not global and apply only to a single channel should be sent following the Select Channel command.

2. Commands that are mode-dependent should be sent only after the mode has been defined with the Main Mode command.

3. Commands that do not define the data access mode should only be sent while the receiver is disabled.

NOTE: Any of the commands listed as required are only required if it is desired to change the channel from its current or default settings.

Command Descriptions

A detailed description of each command, in alphabetical order, is given on the following pages.

Command: BR (Bit Rate)

Syntax: [f/s]BR

Purpose: The BR (Bit Rate) command sets the active channel's receiver to expect data transmission over the ARINC-429 bus at either a slow bit rate (12 to 14.5 kb/s) or a fast bit rate (100 kb/s). For this command to function properly, the active channel's receiver must not be enabled when this command is issued.

Description: [f/s] is a 1-digit decimal integer that specifies the nominal bit rate as follows:

[f/s]	Bit Rate (kb/s)
0	12 - 14.5
1	100

Bit rates outside the 12 to 14.5 Kb/s for the slow rate and outside 90 to 108 Kb/s for the fast rate will result in receiver bit count errors or interword gap errors. If necessary, component modifications may be made to accommodate other bit rates. Please consult the factory for additional information.

On power-up or after an RS (Reset) command, the bit rate for all channels defaults to slow (12-14.5 Kb/s).

Examples:

1. 0BR selects a slow bit rate (12 kb/s to 14.5 kb/s) for the active channel.
2. 1BR selects a fast bit rate (100 kb/s) for the active channel.

Errors: If the active channel's receiver is enabled, a Command Receiving error will result.

A Syntax error will result if an out-of-range value is specified for [f/s].

If either error is generated when the command is received, the command will be ignored.

Command: BT (Block Transfer)

Syntax: [num]BT[labi][mdi]

Purpose: The BT (Block Transfer) command defines a data response list of labels in the All-labels mode for the active channel. Data will be returned for those labels in the order they appear in the list in response to subsequent input requests from the system controller. For this command to function properly, the active channel must be in one of the four All-label modes.

Description: [num] is a 1- to 2-digit decimal integer from 1 to 50 that specifies the number of labels contained in the block transfer.

[labi] is a single character in 8-bit binary format which specifies the ith label whose data is to be returned. The data will be returned in the same order in which labels were loaded for the BT command.

[mdi] is a single character in 8-bit binary format that specifies the secondary capture mode and the SDI and SSM fields, if used. (See the Formats section of this manual for a description of the format for the label and secondary mode byte fields.)

The SDM and SDI mode selection bits in the secondary mode byte are ignored in the All-labels mode (mode selection is determined by the All-labels sub-mode selected by the MM command). The SDM and SDI 2-bit values in the secondary mode byte are only used if an applicable All-labels sub-mode has been programmed.

CAUTION:

A [labi] byte and an [mdi] byte must be sent for the number of label/secondary mode parameters specified by [num]. If fewer bytes than required are sent, subsequent unrelated command characters will be used as label/secondary mode parameters until the required number of bytes is received.

Examples: These definitions apply for all the examples:

lab1 = 023 octal (ADF Frequency)
lab2 = 222 octal (VOR Omnibearing)
lab3 = 125 octal (Greenwich Mean Time)
md1 = 0h
md2 = 01h
md3 = 02h
md4 = 04h
md5 = 08h
md6 = 0Fh

All examples assume no time-stamp/error storage.

See the Secondary Mode Byte Format sub-section for the derivation of SDIn and SSMn values from the mdn values defined for these examples.

Example 1: All-label Mode, Labels Only (see MM command mode 3):
The command string

3BT[lab1][md1][lab2][md2][lab3][md3]

programs the active channel to return data for lab1, lab2, and lab3 in the following sequence:

Data Response Sequence

Byte	Data
1	lab1 label
2-4	lab1 data bytes
5	lab2 label
6-8	lab2 data bytes
9	lab3 label
10-12	lab3 data bytes

Example 2: All-label Mode, Labels and SDI (see MM command mode 4):
The command string

3BT[lab2][md1][lab3][md4][lab1][md5]

programs the active channel to return data for lab2 with SDI2 and SDI1 zero, lab3 with SDI2 = 0 and SDI1 = 1, and lab1 with SDI2 = 1 and SDI1 = 0.

Data Response Sequence

Byte	Data
1	lab2 label
2-4	lab2 data bytes
5	lab3 label
6-8	lab3 data bytes
9	lab1 label
10-12	lab1 data bytes

Example 3: All-label Mode, Labels and SSM (see MM command mode 5):
The command string

3BT[lab2][md1][lab1][md2][lab3][md3]

programs the active channel to return data for lab2 with SSM2 and SSM1 zero, lab1 with SSM2 = 0 and SSM1 = 1, and lab3 with SSM2 = 1 and SSM0 = 0.

Data Response Sequence

Byte	Data
1	lab2 label
2-4	lab2 data bytes
5	lab1 label
6-8	lab1 data bytes
9	lab3 label
10-12	lab3 data bytes

Example 4: All-label Mode, Labels, SDI, and SSM (see MM command mode 6): The command string:

3BT[lab3][md4][lab1][md6][lab1][md1]

programs the active channel to return data for lab3 with SDI2, SSM2, and SSM1 zero, and SDI1 one; lab1 with bits SDI2, SDI1, SSM2, and SSM1 one; and lab1 with SDI2, SDI1, SSM2, and SSM1 all zero.

Data Response Sequence

Byte	Data
1	lab3 label
2-4	lab3 data bytes
5	lab1 label
6-8	lab1 data bytes
9	lab1 label
10-12	lab1 data bytes

Errors: A Syntax error will result if an out-of-range value is specified for [num].

A Command Mode error will result if the active channel is not in one of the four possible All-label modes.

If either error is generated when the command is received, the command will be ignored.

Command: CD (Clear Data)

Syntax: [chan]CD

Purpose: The CD (Clear Data) command clears all of the message RAM for the specified channel or all channels. In addition to clearing stored data for the specified channel(s), the CD command also clears the specified channel's interrupt bit in the byte returned in response to an EX (Examine Status) command, and any unreported interrupts for the specified channels.

Description: [chan] is a 1-digit decimal integer that specifies the following:

[chan]	Channel(s) Cleared
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

The RE (Receiver Enable) command clears message RAM in all modes except the All-label Modes. The CD command is therefore most useful in the All-label Mode to clear memory prior to enabling the receiver to guarantee that the data in memory is valid data. For the All-label mode, data locations for labels 0 through 254 will be cleared to all ones, and label 255 will be cleared to all zeros.

The CD command may be sent when the receiver is enabled, except in the Limit-check Mode.

Examples:

1. 0CD (or simply CD) clears all of the message RAM on the VX4428 receiver.

2. 1CD clears all of the message RAM for channel 1.

Errors: A Syntax error will result if an out-of-range value is specified for [chan].

A Command Receiving error will result if the specified channel is in the Limit-check mode and has not completed data reception.

If a Syntax error is generated when the command is received, the command will be ignored. If a Command Receiving error is generated when the command referencing a single channel is received, the command will be ignored. If a Command Receiving error is generated when the command referencing all channels is received, the command will be executed for all channels in which the error did not occur.

NOTE: This command will not clear interrupts which have already activated the VXIbus interrupt line.

Command: CL (Clear Label)

Syntax: [chan]CL

Purpose: The CL (Clear Label) command clears from memory any previously defined labels (see the LC, LL and SL commands) for the Select-labels Monitor Mode and Limit-check Mode, for the specified channels. For this command to function properly, the specified channel(s) must be in the Select-labels Monitor Mode or Limit-check Mode with their receivers disabled.

Description: [chan] is a 1-digit decimal integer that specifies the following:

[chan]	Channel(s) Cleared
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

On power-up or following an RS (Reset) command, all labels are cleared.

Examples:

1. 0CL (or simply CL) clears the capture labels for all the channels.

2. 1CL clears the capture labels for channel 1.

Errors: A Syntax error will result if an out-of-range value is specified for [chan].

A Command Receiving error will result if a specified channel(s)'s receiver is enabled.

A Command Mode error will result if the specified channel(s) is not in Select-labels Monitor Mode or Limit-check Mode.

If a Syntax error is generated when the command is received, the command will be ignored. If a Command Receiving or Command Mode error is generated when the command referencing a single channel is received, the command will be ignored. If a Command Receiving or Command Mode error is generated when the command referencing all channels is received, the command will be executed for all channels in which the error did not occur.

Command: DS (Data Storage)

Syntax: [type]DS

Purpose: The DS (Data Storage) command specifies the type of data words to be stored for the active channel. For this command to function properly, the active channel's receiver must be disabled.

Description: [type] is a 1-digit decimal integer that specifies the type of data words stored as follows:

[type]	Type of Data Words Stored
0	Labels and data only.
1	Labels and data, plus time-stamp and error bytes.
2	Only those data words in which errors are detected, plus time-stamp and error bytes for those words.

In addition to changing the data storage type, the DS command also clears the memory for all modes except the All-label modes, clears the active channel's status bits in the byte returned in response to an EX (Examine Status) command, and any unreported interrupts for the active channel, and clears the pre-trigger and post-trigger values for the Limit-check Mode.

On power-up or after an RS (Reset) command, the data storage mode defaults to a "1DS" - labels and data, plus time-stamp and error bytes.

NOTE: This command will not clear the interrupt for the active channel if the interrupt has activated the VXIbus interrupt line.

Errors: A Syntax error will result if an out-of-range value is specified for [type].

A Command Receiving error will result if the active channel's receiver is enabled.

If either error is generated when the command is received, the command will be ignored.

Command: ER (Error Return)

Syntax: ER

Purpose: The ER (Error Return) command will cause the codes of any errors encountered during the use of the VX4428 receiver to be returned in response to subsequent input requests to the module. Each returned error code consists of two ASCII characters, followed by <CR><LF>.

Description: After the ER command is issued, the VX4428 receiver will continue to return error codes until the error code 99 (no additional errors to report) is returned. Additional requests for input after error code 99 is returned will cause the VX4428 receiver to return data for the active channel in the currently selected data-return mode (see the SD command).

If an ER command is issued and no errors are found, only error code 99 is returned. Because the error buffer can store a maximum of 16 errors, only the first 16 errors are returned; any additional errors are lost. Errors are returned in the order in which they occurred.

Each error code is returned as two ASCII characters followed by <CR><LF>.

NOTE: Issuing the CD, DS, MM, SC, or SD command before receiving error code 99 will cause the VX4428 receiver to cease returning error codes and return to the previously selected data return mode for the selected channel.

ERROR CODES

Fatal Errors:

"Fatal" errors cause the VX4428 receiver to disable the ARINC receiver inputs. The VX4428 receiver accepts commands from the system controller, but will not perform functions for any commands. Any input from the module will return only the error code for the fatal error:

Error Code		
Char 1	Char 2	Description
0	0	RAM failure
0	1	(Reserved)
0	2	Interrupt-controller failure
0	3	(Reserved)
0	4	General hardware failure

Nonfatal Errors:

"Nonfatal" errors do not cause the VX4428 receiver to totally suspend its operations. However, a hardware error (error code X3) within a channel disables data reception on that channel until the hardware error is cleared.

Error Code Char 1	Char 2	Description
X	0	Unrecognized command
X	1	Syntax error
X	2	(Reserved)
X	3	ARINC-receiver error (hardware)
X	4	Memory overflow
X	5	Command receiving error. Invalid command while channel is receiving data.
X	6	Command mode error. Invalid command for mode selected.
9	9	No additional errors to report.

X = Number of the channel in which the error occurred.

The ER command does not clear the channel ERR LEDs (see EX command). The main ERR LED, if set, will be cleared after error code 99 is returned.

Example: Following an ER command, the following responses are returned:

21 <CR><LF>
99 <CR><LF>

These responses indicate one error has occurred since the last input request, a programming syntax error in channel 2.

Command: EX (Examine Status)

Syntax: EX

Purpose: The EX (Examine Status) command will cause the interrupt/status byte to be returned in response to the next input request to the module.

Description: The status is read back as one byte in 8-bit binary format followed by <CR><LF>. The status byte has the following format:

Bit Position	7	6	5	4	3	2	1	0
Bit Definition	ERR4	INT4	ERR3	INT3	ERR2	INT2	ERR1	INT1

INT1, INT2, INT3, AND INT4 Bits

INT1 through INT4 indicate when an interrupt condition has been met for channel 1 through channel 4, respectively, if interrupts have not been enabled with the IN command. If interrupts have been enabled, the channel's interrupt condition will be returned through the VXIbus Word Serial command Read STB, and not through the EX command. Reading the status byte will clear the interrupt bit in the status byte.

ERR1, ERR2, ERR3, and ERR4 Bits

ERR1 through ERR4 indicate when a received data error has been detected for channel 1 through channel 4, respectively. Reading the status byte will cause the error LEDs to go out for each channel reporting an error.

Example: Following an EX command, the following response is returned:

h14 <CR><LF>

This returned byte with a hexadecimal value of 14 indicates that channels 2 and 3 have satisfied their interrupt conditions.

Errors: A Syntax error will result if a parameter value precedes the command.

If a Syntax error is generated when the command is received, the command will be ignored.

Command: ID (Return ID)

Syntax: ID

Purpose: The ID (Return ID) command will cause the VX4428 receiver to return a string containing the module identification and software version to the system controller on its next request for input from the card.

Description: The string returned by this command is:

CDS VX4428 RECEIVER VX.X<CR><LF>

where X.X represents the version of the software.

The ID command will be aborted by receiving a M command or the VXIbus word serial Clear command.

NOTE: Issuing the CD, DS, MM, SC, or SD command before receiving the <CR><LF> will cause the VX4428 receiver to abort the ID command and return to the previously selected data return mode for the active channel.

Errors: A Syntax error will result if a parameter value precedes the command.

If a Syntax error is generated when the command is received, the command will be ignored.

Command: IN (Interrupt)

Syntax: [e/d]IN

Purpose: The IN (Interrupt) command enables or disables interrupts from the VX4428 receiver to the system controller for the active channel.

Description: [e/d] is a 1-digit decimal integer that specifies the following:

[e/d]	Action
0	Interrupts are disabled.
1	Interrupts are enabled.

If interrupts are enabled, interrupts are conditionally generated by the VX4428 receiver for each channel, depending on the selected mode:

1. In Monitor Mode or Select-labels Monitor Mode, interrupts are generated when the memory becomes 3/4 full. This interrupt is provided so that new data will not be lost when the memory becomes completely full.

2. In Limit-check Mode, interrupts are generated when the received data meets a limit condition (see the LP command) and the preset number of bytes have been stored (see the PT and PR commands).

If the IN command is programmed while an interrupt condition is already active on the selected channel, the interrupt condition will be handled as follows:

If the IN command enables interrupts which were previously disabled for the active channel and if an interrupt condition has been met for the active channel, then the active channel's Interrupt bit will be cleared in the byte returned in response to an EX (Examine Status) command, and an interrupt will be generated as soon as any presently active interrupts have been acknowledged.

If the IN command disables interrupts which were previously enabled for the active channel and if an interrupt has been generated which is unreported (has not yet activated the VXIbus interrupt line), then the channel's Interrupt bit in the byte returned in response to an EX (Examine Status) command will be set and the unreported interrupt will be cleared.

On power-up or after an RS (Reset) command, interrupts are disabled.

Example: 0IN disables interrupts.

Errors: A Syntax error will result if an out-of-range value is specified for [e/d].

If a Syntax error is generated when the command is received, the command will be ignored.

Command: LC (Label Change)

Syntax: [addr]LC[lb][md]

Purpose: The LC (Label Change) command selectively changes one label in the list of six capture labels in Select-labels Monitor Mode for the active channel. For this command to function properly, the active channel must be in the Select-labels Monitor Mode with its receiver disabled.

Description: [addr] is a 1-digit decimal integer, from 1 to 6, that specifies which of the six labels to change in Select-labels Monitor Mode.

[lb] is a single character in 8-bit binary format which specifies the value for the new label.

[md] is a single character in 8-bit binary format which specifies the secondary capture mode for the new label.

See the Formats subsection of this manual for a description of the format for the [lb] label and [md] secondary mode bytes.

NOTE: In the following examples the [lb] and [md] parameters will be shown as hexadecimal characters. The examples should not be copied directly as shown as an ASCII string. The parameters are only representative of the required 8-bit byte.

Examples: In the following examples, it is assumed that labels were previously loaded using the LL command.

1. 2LC[13][00] sets the label at address 2 in the 6-label list to octal 023, and sets the secondary capture mode for Label 2 to capture data based on the label only. Hexadecimal 13 is equivalent to octal 023.

2. 4LC[55][88] sets the label at address 4 in the 6-label list to octal 125, and sets the secondary capture mode for Label 4 to capture data based on the label with the SDI field having a value of binary 10.

3. 16LC[92][42] sets the label at address 6 in the 6-label list to octal 222, and sets the secondary capture mode for Label 6 to capture data based on the label with the SSM field having a value of binary 10.

Errors: A Syntax error will result if an out-of-range value is specified for [addr] or if the label address has not been previously loaded with the LL command.

A Command Mode error will result if the active channel is not in the Select-labels Monitor Mode.

A Command Receiving error will result if the active channel's receiver is enabled.

Command: LL (Load Labels)

Syntax: [num]LL[labi][mdi]

Purpose: The LL (Load Labels) command specifies a set of labels and secondary capture modes in Select-labels Monitor Mode for the active channel. For this command to function properly, the active channel must be in the Select-labels Mode with its receiver disabled.

Description: [num] is a 1-digit decimal integer from 1 to 6 that specifies the number of label/mode pairs to be stored. The label/mode pairs will be stored in memory in the same sequence in which they are sent (the first pair will be stored at label address 1, the second pair at label address 2, etc.). The label address from 1 to 6 is used to selectively change a single label later with the LC (Label Change) command.

[labi] is a single character in 8-bit binary format which specifies the value of the ith label to be captured.

[mdi] is a single character in 8-bit binary format which specifies the secondary capture mode for the ith label.

See the Formats subsection of this manual for a description of the format for the [labi] label and [mdi] secondary mode fields.

CAUTION:

A [labi] byte and an [mdi] must be sent for the number of label/secondary mode parameters specified by [num]. If fewer bytes than required are sent, subsequent unrelated command characters sent to this module will be misinterpreted as the completion of this command, resulting in incorrect operation of the VX4428 receiver.

NOTE: In the following examples the [lb] and [md] parameters will be shown as hex characters. The examples should not be copied directly as shown as an ASCII string. The parameters are only representative of the required 8-bit byte.

Examples:

1. 1LL[40][00] sets the number of labels to capture to one with the label set to octal 100, and sets the secondary capture mode for the label to capture data based on the label only. This label will have a label address of 1.

2. 2LL[55][88][13][00] sets the number of labels to capture to two. The label at address 1 is set to octal 125, and the secondary capture mode for the first label will capture data based on the label with the SSM field having a value of binary 10. The label at address 2 is set to octal 023; and the secondary capture mode for the second label will capture data based on the label only.

Errors:

A Syntax error will result if an out-of-range value is specified for [num].

A Command Mode error will result if the active channel is not in the Select-labels Monitor Mode.

A Command Receiving error will result if the active channel's receiver is enabled.

If any of these errors is generated when the command is received, the command will be ignored.

Command: LM (Load Monitor Mode Masks)

Syntax: [num];{[ldbyt]}LM[byts]

Purpose: The LM (Load Monitor Mode Masks) command specifies a set of data words to be used by the Monitor Mode to generate trigger outputs for the active channel. For this command to function properly, the active channel must be in the Monitor Mode with its receiver disabled.

Description: The LM command sets up a list of comparison masks for received messages that generate a trigger output when the received data matches any of the comparison masks. Each mask can be set up to compare on any combination of the four bytes contained in a received message.

[num] is a 1-digit decimal integer from 1 to 6 that specifies the number of ARINC word data sets to be stored. The data sets will be stored in memory in the same sequence in which they are sent.

A value of 0 or a blank value for the [num] parameter will clear all of the Monitor Mode data sets in memory.

The [ldbyt] parameter is used to indicate which bytes are to be loaded and used for comparison in a message mask. The number of [ldbyt] parameters present in the LM command must be equal to the [num] parameter.

Each byte is represented by a 1-digit decimal integer from 1 to 4. The values correspond the byte position within the ARINC word (1 indicates the first byte of the received message, 2 the second byte, etc.).

Each byte indicator within the [ldbyt] parameter must be separated from the following indicator by a comma (,).

Example : 1,2,3,4

There must be a minimum of 1 byte and a maximum of 4 bytes defined within the [ldbyt] parameter.

Each [ldbyt] parameter must be separated from a following [ldbyt] parameter by a colon (;).

Example : 1;2,3;4

The LM command will erase all existing masks when the command completes execution.

[byts] is a single character in 8-bit binary format which specifies the value to be used for the comparison masks. Each byte defined for comparison in the [ldbyt] parameter must have a corresponding [byts] parameter in the same order.

The format of each byte to match a specific ARINC word bit position can be determined by using the label/data read format. (See the Formats subsection of this manual for a description of the format label/data read.) Each specific byte being defined matches a byte defined by this format.

CAUTION:

The required number of [byts] bytes for the number of masks and bytes as specified by the [ldbyt] parameters. If fewer bytes than required are sent, subsequent unrelated command characters sent to this module will be misinterpreted as the completion of this command, resulting in incorrect operation of the VX4428 receiver.

NOTE: In the following examples the [byts] parameters will be shown as hex characters. The examples should not be copied directly as shown as an ASCII string. The parameters are only representative of the required 8-bit byte.

Examples:

1. 0LM or LM will clear all of the comparison masks stored in memory.

2. 1;1LM[55] will cause the active channel to generate a trigger output when the first byte of a received message is equal to 55 hex.

3. 4;1;2;3;4LM[33][AA][01][7F] will cause the active channel to generate a trigger output under any of the following conditions:

   a. The first byte of a received message is equal to 33 hex.

   b. The second byte of a received message is equal to AA hex.

   c. The third byte of a received message is equal to 01 hex.

   d. The fourth byte of a received message is equal to 7F hex.

Errors:

A Syntax error will result if an out-of-range value is specified for [num].

A Syntax error will result if an out-of-range value is specified for [ldbyt].

A Command Mode error will result if the active channel is not in the Monitor Mode.

If any of these errors is generated when the command is received, the command will be ignored.

Command: LP (Limit Parameters)

Syntax: [comp]LP[lim]

Purpose: The LP (Limit Parameters) command defines the value of the limit parameter and the type of comparison used for the trigger event in the Limit-check Mode for the active channel. For this command to function properly, the active channel must be in the Limit-check Mode with its receiver disabled.

Description: [comp] is a 1-digit decimal integer that specifies the type of comparison used for the trigger event as follows:

[comp]	Trigger Event
1	Received data = [lim].
2	Received data < [lim] (binary comparison).
3	Received data > [lim] (binary comparison).

> = or < = functions may be performed by increasing or decreasing the limit value by 1.

[lim] has three characters in 8-bit binary format which specifies the limit to be checked for. (See the Formats subsection of this manual for the format of the Limit Bytes, and handling of Bit 32 and the SDI and SSM bits). In addition to loading the limit parameter, the LP command also clears the memory, clears the active channel's Status bits in the byte returned in response to an EX (Examine Status) command, and any unreported interrupts for the active channel, and clears the pre-trigger and post-trigger values for the Limit-check Mode.

After the Limit-check trigger event has occurred, data reception and storage will cease after the number of words set by the Post-Trigger (PT) command have been received.

CAUTION:

If these bytes are not sent following the LP characters, unrelated command characters sent to this module will be misinterpreted as the completion of this command, resulting in incorrect operation of the VX4428 receiver.

NOTE: This command will not clear the interrupt for the active channel if the interrupt has been activated by the VXIbus interrupt line.

Example: The following examples assume that the receiver's active channel is in Limit-check mode.

1. This example assumes that a capture label has been loaded using the SL command as follows: SL[13][00]

The command

1 LP [00][00][7F]

will cause the Limit-check trigger event to occur when the data for label 13h has bits 31-25 equal to 1's and all other bits zero.

2. This example assumes that a capture label has been loaded using the SL command as follows: SL[13][88]

The command

1 LP [FC][00][00]

will cause the Limit-check trigger event to occur when the following conditions are met:

label = 13h
data 9 = 0; 10 = 1 (SDI bits)
data bits 11-31 must be less than the following value:
00000000000000111111b

Errors: A Syntax error will result if an out-of-range value is specified for [comp].

A Command Mode error will result if the active channel is not in the Limit-check Mode.

A Command Receiving error will result if the active channel's receiver is enabled.

If any of these errors is generated when the command is received, the command will be ignored.

Command: MM (Main Mode)

Syntax: [mode]MM

Purpose: The MM (Main Mode) command selects one of the four primary capture modes for the active channel, and for the All-labels mode, selects one of the four sub-modes. For this command to function properly, the active channel's receiver must be disabled.

Description: [mode] is a 1-digit decimal integer that specifies the primary capture mode as follows:

[mode]	Primary Capture Mode
0	Monitor Mode
1	Select-labels Monitor Mode
2	Limit-check Mode
3	All-label Mode Labels Only
4	All-label Mode Labels and SDI
5	All-label Mode Labels and SSM
6	All-label Mode Labels, SDI, and SSM

The All-label Mode is programmed as one of four sub-modes to permit proper partitioning of memory for maximum data transfer rate performance.

To clear memory for the All-label Mode the Clear Data (CD) command must be used.

In addition to changing the main mode, the MM command also clears the memory for all modes except the All-label Modes, clears the active channel's status bits in the byte returned in response to an EX (Examine Status) command, and any unreported interrupts for the active channel, and clears the pre-trigger and post-trigger values for the Limit-check Mode.

NOTE: This command will not clear the interrupt for the active channel if the interrupt has been activated by the VXIbus interrupt line.

Example: The command 4MM selects the All-labels mode for the active channel and specifies that separate memory locations will be provided for storage of each SDI value for each label. Four 'mailbox' locations will be set aside for each of the 256 labels corresponding to the four possible values of the SDI bits (bits 10 and 9) of the ARINC-429 word. See the BT command description and the Formats

section of this manual for a description of the secondary mode byte format to determine how to access the data in these 'mailboxes'.

Errors: A Syntax error will result if an out-of-range value is specified for [mode].

A Command Receiving error will result if the active channel's receiver is enabled.

If either of these errors is generated when the command is received, the command will be ignored.

Command: PR (Pre-Trigger)

Syntax: [num]PR

Purpose: The PR (Pre-Trigger) command specifies the number of words to store prior to the trigger event in the Limit-check Mode for the active channel. For this command to function properly, the active channel must be in the Limit-check Mode with its receiver disabled.

Description: [num] is a 1- to 5-digit decimal integer specifying the number of words to capture before the trigger condition has been met. [num] has a value from 0 to 31999 for data storage without time-stamp error bytes, and 0 to 15999 for data storage with time-stamp error bytes.

Example: 100PR sets the number of words to be stored before the trigger event has occurred to 100 words.

Errors: A Syntax error will result if an out-of-range value is specified for [num].

A Command Receiving error will result if the active channel's receiver is enabled.

A Command Mode error will result if the active channel is not in the Limit-check mode.

If any of these errors is generated when the command is received, the command will be ignored.

Command: PT (Post-Trigger)

Syntax: [num]PT

Purpose: The PT (Post-Trigger) command specifies the number of words to store following the trigger event for the Limit-check Mode for the active channel. For this command to function properly, the active channel must be in the Limit-check Mode with its receiver disabled.

Description: [num] is a 1- to 5-digit decimal integer specifying the number of words to capture after the trigger event. [num] has a value from 0 to 31999 for data storage without time-stamp/error bytes, and 0 to 15999 for data storage with time-stamp/error bytes.

Examples:

1. 100PT sets the number of words to be stored after the trigger event has occurred to 100 words.

2. 200PR2000PT sets the number of words to be stored prior to the trigger event to 200 words and following the event to 2000 words. After data collection is completed, these 2200 words plus the trigger word will be returned as a 2201 word circular buffer in response to repeated input requests.

Errors: A Syntax error will result if an out-of-range value is specified for [num].

A Command Receiving error will result if the active channel's receiver is enabled.

A Command Mode error will result if the active channel is not in the Limit-check mode.

If any of these errors is generated when the command is received, the command will be ignored.

Command: RC (Relay Close)

Syntax: [chan]RC

Purpose: The RC (Relay Close) command will close the source selection relays to connect the receivers to the input connector for the specified channel(s).

Description: [chan] is a 1-digit decimal integer (or blank) that specifies the channel or channels affected by the RC command as follows:

[chan]	Channel(s) Affected
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

NOTE: After the RO command has been executed, there will be a 10 millisecond delay to allow the relays to settle before the module will be ready for subsequent commands.

CAUTION:

The relays can be opened (with the RO command) or closed (with the RC command) with the receivers enabled. If the relays change position while data transmission is occurring on the DITS bus, received data corruption may occur. It is recommended that the Relay Close command be used only while data transmission is not occurring.

Examples:

1. RC or 0RC will connect all four channels to the main input connectors.
2. 1RC will connect channel 1 to the input connector.
3. 2RC will connect channel 2 to the input connector.
4. 3RC will connect channel 3 to the input connector.
5. 4RC will connect channel 4 to the input connector.

Errors: A Syntax error will result if an out-of-range value is specified for [chan].

If a Syntax error is generated when the command is received, the command will be ignored.

Command: RD (Receive Disable)

Syntax: [chan]RD

Purpose: The RD (Receive Disable) command disables data reception for the specified channel(s).

Description: [chan] is a 1-digit decimal integer (or blank) that specifies the following:

[chan]	Channel(s) Disabled
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

NOTE: The RD command does not destroy the data already stored in memory. The data stored in memory is still accessible by the system controller.

NOTE: If the RD command is issued to a channel in the Limit-check Mode before data collection is complete, in addition to disabling the receiver, an adjustment is made on the amount of available response data. The data adjustment is based on the pre-trigger value, the post-trigger value, the number of words received, and on whether the comparison limit has been met, as follows:

IF WS > PTV + PRV + CP
THEN NW = PTV + PRV + CP
ELSE NW = WS

where:

WS = Number of words stored
PTV = Post-trigger value
PRV = Pre-trigger value
CP = 1 if the comparison limit has been met;
0 if the comparison limit has not been met
NW = Number of words available for read-back

Examples:

1. 0RD (or simply RD) disables data reception on all four channels.

2. 2RD disables data reception on channel 2.

Errors: A Syntax error will result if an out-of-range value is specified for [num].

If a Syntax error is generated when the command is received, the command will be ignored.

Command: RE (Receiver Enable)

Syntax: [chan]RE

Purpose: The RE (Receiver Enable) command enables data reception for the specified channel(s).

Description: [chan] is a 1-digit decimal integer (or blank) that specifies the following:

[chan]	Channel(s) Enabled
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

In addition to enabling the receiver, the RE command also clears the memory for all modes except the All-label modes, clears the active channel's Status bits in the byte returned in response to an EX (Examine Status) command, and any unreported interrupts for the active channel, and clears the pre-trigger and post-trigger values for the Limit-check Mode, and clears the channel's Error LED.

Data reception also requires the source selection relay for the channel to be closed prior to the RE command (see the RC command).

NOTE: This command will not clear the interrupt for the active channel if the interrupt has been activated by the VXIbus interrupt line.

Examples:

1. 4RE enables channel 4 to receive data.

2. 0RE (or simply RE) enables all four channels to receive data.

Errors: A Syntax error will result if an out-of-range value is specified for [chan].

If a Syntax error is generated when the command is received, the command will be ignored.

Command: RO (Relay Open)

Syntax: [chan]RO

Purpose: The RO (Relay Open) command will open the source selection relays to connect the receivers to the VX4428 self-test data path for the specified channel(s).

Description: [chan] is a 1-digit decimal integer (or blank) that specifies the channel or channels affected by the RO command as follows:

[chan]	Channel(s) Affected
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

NOTE: After the RO command has been executed, there will be a 10 millisecond delay to allow the relays to settle before the module will be ready for subsequent commands.

CAUTION:
The relays can be opened (with the RO command) or closed (with the RC command) with the receivers enabled. If the relays change position while data transmission is occurring on the DITS bus, received data corruption may occur. It is recommended that the Relay Close command be used only while data transmission is not occurring.

Examples:

1. RO or 0RO will connect all four channels to the self-test data path.
2. 1RO will connect channel 1 to the self-test data path.
3. 2RO will connect channel 2 to the self-test data path.
4. 3RO will connect channel 3 to the self-test data path.
5. 4RO will connect channel 4 to the self-test data path.

Errors: A Syntax error will result if an out-of-range value is specified for [chan].

If a Syntax error is generated when the command is received, the command will be ignored.

Command: RS (Reset)

Syntax: RS

Purpose: The RS (Reset) command stops the receiver operation and returns the VX4428 receiver to its power-up state. It does not affect the VXIbus interface. See the Specifications section of the manual for a listing of the power-up status.

Errors: A Syntax error will result if a parameter precedes the command.

If a Syntax error is generated when the command is received, the command will be ignored.

Command: SC (Select Channel)

Syntax: [chan]SC

Purpose: The SC (Select Channel) command selects a channel to be the active channel for subsequent commands.

Description: [chan] is a 1-digit decimal integer that specifies the following:

[chan]	Channel Selected
1	1
2	2
3	3
4	4

Note that if this command is issued to change the selected channel prior to the completion of a multi-word transfer, the present data return location for the Monitor Mode, Select-labels Monitor Mode, or Limit-check Mode will be saved, so that data access may be resumed from that point when the channel is re-selected.

Example: 3SC selects channel 3 to be the active channel for subsequent commands from the system controller.

Errors: A Syntax error will result if an out-of-range value is specified for [chan].

If a Syntax error is generated when the command is received, the command will be ignored.

Command: SD (Select Data)

Syntax: [mode][num]SD

Purpose: The SD (Select Data) command specifies the data input mode for return of data words to the system controller from the active channel. It is for use in the Monitor and Label-select Monitor modes and in the Limit-check mode after capture is complete.

Description: [mode] is a 1-digit decimal integer that specifies the data-return mode as follows:

[mode]	Quantity of Data Returned
0	Single word
1	Number of ARINC-429 data words specified by [num]
2	All available data

On completion of [mode] = 1 or 2, the selected channel reverts to [mode] = 0.

[num] is a 1- to 5-digit decimal integer (used in mode 1 only), from 1 to 32000 (from 1 to 16000 with time-stamp and error bytes stored), that specifies the number of data words to be returned. Returned data will start at the next word to be read from memory. If [num] is greater than the number of data words stored, then all of the currently stored data words will be returned. The data input mode will then return to mode 0.

NOTE: When [mode] = 0 or 2 the parameter [num] should not be sent.

The 0SD command is not necessary to start data transfers. Its intended use is to abort modes 1 and 2.

In the All-labels Mode, modes 1 and 2 cannot be used. In the Limit-check Mode, modes 1 and 2 cannot be used until the active channel has completed data capture.

See the Data Access subsection in the Operation section of this manual for more information on the operation of the three data access modes, including information on termination of data and system controller use.

Examples: These examples assume that the active channel is in Select-labels Monitor Mode.

1. 0SD sets the active channel on the VX4428 receiver to return the next stored word in response to an input request from the system controller. Every input request will return the next word stored in memory.

2. 122SD sets the active channel on the VX4428 receiver to return the next 22 stored words for the selected label in response to an input request from the system controller.

3. 2SD sets the active channel on the VX4428 receiver to return all stored data words in response to an input request from the system controller. The first two bytes (each byte is 8-bit binary) returned will contain the number of data words being returned, with the first byte being the low byte and the second byte being the high byte.

Errors: A Syntax error will result if an out-of-range value is specified for [mode] or [num].

A Command Receiving error will result if the active channel is in the Limit-check Mode, has not completed data storage, and the [mode] parameter for this command is 1 or 2.

A Command Mode error will result if the active channel is in the All-label Mode, and the [mode] parameter for this command is 1 or 2.

If any of these errors is generated when the command is received, the command will be ignored.

Command: SL (Set Labels)

Syntax: SL[lb][md]

Purpose: The SL (Set Label) command defines the Limit-check Mode capture label for the active channel. For this command to function properly, the active channel must be in the Limit-check Mode with its receiver disabled.

Description: [lb] is a single character in 8-bit binary format that specifies the value for the label.

[md] is the secondary capture mode for the label.

See the Activity Modes subsection of this manual for a description of the format of the [lb] and [md] bytes.

CAUTION:

If two bytes are not sent following the SL command, one for the label and one for the secondary capture mode, subsequent unrelated commands will be interpreted as the two required bytes,causing improper operation of the module.

NOTE: In the following examples the [lb] and [md] parameters will be shown as hex characters. The examples should not be copied directly as shown as an ASCII string. The parameters are only representative of the required 8-bit byte.

Examples:

1. SL[13][00] sets the label to capture to octal 023 and sets the secondary capture mode to capture based on the label only. Hexadecimal 13 is equivalent to decimal 19.

2. SL[55][88] sets the label to capture to octal 125, and sets the secondary capture mode to capture based on the label and the SDI field having a value of binary 10.

3. SL[92][42] sets the label to capture to octal 222 and sets the secondary capture mode to capture based on the label and the SSM field having a value of binary 10.

Errors: A Syntax error will result if any parameter values precede the command.

A Command Receiving error will result if the active channel's receiver is enabled.

A Command Mode error will result if the active channel is not in the Limit-check Mode.

If any of these errors is generated when the command is received, the command will be ignored.

Command: ST (Self Test)

Syntax: ST

Purpose: The ST (Self Test) command is used to perform a complete self test of the VX4428 receiver.

Description: The error codes for any errors found can be read by using the ER command. When this self test is complete, the VX4428 receiver will be returned to its power-up state. This command does not affect the VXIbus interface. (See the Specifications section of the manual for a listing of the power-up status.)

The supplied self test also does not test the ARINC-429 interface. The self test data path may be used with VX4428 transmitter to create a wrap-around test and test procedure which tests both modules while isolating both modules from the UUT.

Errors: A Syntax error will result if any parameter values precede the command.

If a Syntax error is generated when the command is received, the command will be ignored.

Command: TD (Terminate Data)

Syntax: [crlf]TD

Purpose: The TD (Terminate Data) command defines whether or not <CR><LF> is appended to the end of a data transfer for the active channel.

Description: [crlf] is a 1-digit decimal integer that specifies the following:

[crlf]	Action
0	<CR><LF> is not appended to the end of either block or single-word data transfers.
1	<CR><LF> is appended to the end of block transfers. <CR><LF> is appended to the end of single-word transfers if no new data is available.

NOTE: In Limit-check Mode, <CR><LF> will not be appended to single word transfers. If selected in other modes, <CR><LF> will only be appended to block transfers.

See the Data Access, Termination Characters, and Termination of Input with the System Controller sub-sections for additional information on termination characters and their use.

Example: The command 0TD suppresses the <CR><LF> termination characters on all responses from the VX4428 receiver to the system controller.

Command: TE (Trigger output Enable)

Syntax: [chan][sel]TE

Purpose: The TE (Trigger output Enable) command defines whether the front panel and/or the backplane trigger output lines will be enabled/disabled for the specified channel(s). The trigger signal is available in the Limit-check mode and is generated when the Limit-check trigger event occurs and the specified number of *ARINC-429 words have been collected.

Description: [chan] is a 1-digit decimal integer (or blank) that specifies the channel or channels affected by the TE command as follows:

[chan]	Channel(s) Enabled
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

[sel] is a 1-digit decimal integer which specifies the enable status of the backplane and front panel trigger generation capability for the specified channel(s) as follows:

[sel]	Action
0	Both the front panel and backplane trigger generation capability are disabled for the specified channel(s).
1	Backplane trigger generation capability is enabled and front panel trigger generation is disabled for the specified channel(s).
2	Front panel trigger generation is enabled and backplane trigger generation is disabled for the selected channel(s).
3	Both front panel and backplane trigger generation are enabled for the specified channel(s).

Use the TS command to specify any of four front panel triggers or any of the VXIbus backplane TTLTRG lines.

NOTE: If the [chan] parameter is used, the [sel] must be included in the command string.

Examples:

1. TE or 00TE disables both the front panel and backplane trigger generation capability for all four channels.

2. 1TE or 01TE enables the backplane and disables the front panel trigger generation capability for all four channels.

3. 2TE or 02TE enables the front panel and disables the backplane trigger generation capability for all four channels.

4. 3TE or 03TE enables both the front panel and backplane trigger generation capability for all four channels.

5. 10TE disables both the front panel and backplane trigger generation capability for channel 1.

6. 21TE enables the backplane and disables the front panel trigger generation capability for channel 2.

7. 32TE enables the front panel and disables the backplane trigger generation capability for channel 3.

8. 43TE enables both the front panel and backplane trigger generation capability for channel 4.

Errors: A Syntax error will result if an out-of-range value is specified for [chan] or [sel].

If a Syntax error is generated when the command is received, the command will be ignored.

Command: TS (Trigger Line Select)

Syntax: [chan]TS[frtrg][bcktrg]

Purpose: The TS (Trigger line Select) command defines which of the trigger output lines for the front panel and the backplane trigger output lines will be used by the specified channel(s). The trigger signal is available in the Limit-check mode and is generated when the Limit-check trigger event occurs and the specified number of ARINC-429 words have been collected.

Description: [chan] is a 1-digit decimal integer (or blank) that specifies the channel or channels affected by the TE command as follows:

[chan]	Channel(s) Enabled
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

[frtrg] is a single character in 8-bit binary format which specifies which front panel trigger lines the specified channel(s) will connected to when the channel(s) front panel trigger generation capability is enabled. The format of the 8-bit byte is as follows:

Bit Position	7	6	5	4	3	2	1	0
	Front panel trigger line(s) selected							
	X	X	X	X	3	2	1	0

Each bit when set will select the indicated trigger as the output for the selected channel. The character X in the above indicates a bit which is not used and therefore whose value has no effect on the trigger line selection.

[bcktrg] is a single character in 8-bit binary format which specifies which backplane trigger lines the specified channel(s) will connected to when the channel(s) front panel trigger generation capability is enabled. The format of the 8-bit byte is as follows:

Bit Position	7	6	5	4	3	2	1	0
	Backplane TTL trigger line(s) selected							
	7	6	5	4	3	2	1	0

Each bit when set will select the indicated trigger as the output for the selected channel.

CAUTION:

Both the [frtrg] and [bcktrg] character bytes are required following the TS command. If these two bytes do not follow the command, subsequent unrelated command characters will be used to complete the command, causing improper operation of the module.

NOTE: In the following examples the [frtrg] and [bcktrg] parameters will be shown as hex characters. The examples should not be copied directly as shown as an ASCII string. The parameters are only representative of the required 8-bit byte.

Examples:

1. TS[00][01] or 0TS[00][01] will select the backplane trigger line 0 as the destination for all four channels trigger output when triggers are enabled.

3. 1TS[03][07] will select the front panel trigger lines 0 and 1 and the backplane trigger lines 0, 1, and 2 as the destination for channel 1's trigger output when triggers are enabled.

4. 2TS[0F][FF] will select all of both the front panel backplane trigger lines as the destination for channel 2's trigger output when triggers are enabled.

5. 3TS[00][00] will select none of both the front panel backplane trigger lines as the destination for channel 3's trigger output when triggers are enabled. This has the same effect as disabling the trigger generation capability for channel 3 (see the TE command).

6. 4TS[08][77] will select the front panel trigger line 3 and the backplane trigger lines 6, 5, 4, 2, 1, and 0 as the destination for channel 4's trigger output when triggers are enabled.

These examples demonstrate the flexibility and range of use of the trigger lines. Typical applications will use a single front panel or single VXIbus TTLTRG line for a specified channel.

Errors:

A Syntax error will result if an out-of-range value is specified for [chan].

If a Syntax error is generated when the command is received, the command will be ignored.

Command: TR (Time-stamp Resolution)

Syntax: [res]TR

Purpose: The TR (Time-stamp Resolution) command sets the time-stamp resolution for all four channels.

Description: [res] is a 1-digit decimal integer that specifies the time-stamp resolution as follows:

[res]	Time-stamp Resolution
0	10 µs
1	100 µs
2	1 ms
3	10 ms
4	100 ms

The time-stamp resolution is multiplied by the time-stamp value to determine the actual time values. (See the subsection on Time-stamp Bytes for additional details.)

The time-stamp value is set to 0 when a receiver channel is enabled. Independent counters are provided for each channel, but they must all be programmed for the same resolution.

Examples:

1. 0TR sets all four channels to time-stamp in 10-µs steps.
2. 3TR sets all four channels to time-stamp in 10-ms steps.

Errors: A Syntax error will result if an out-of-range value is specified for [res].

A Command Receiving error will result if any channel's enabled receiver is in the time-stamp/error storage mode.

If either error is generated when the command is received, the command will be ignored.

SYSFAIL, Self Test, And Initialization

The VX4428 Module will execute a self test at power-up, or upon direction of a VXIbus hard or soft reset condition, or upon command. A VXIbus hard reset occurs when another device, such as the VXIbus Resource Manager, asserts the backplane line SYSRST*. A VXIbus soft reset occurs when another device, such as the VX4428's commander, sets the Reset bit in the VX4428's Control register.

At power-up, as well as during self test, all transmitter outputs and receiver inputs remain isolated from the module's main front panel connector.

During a power-up, or hard or soft reset, the following actions take place:

1) The SYSFAIL* (VME system-failure) line is set active, indicating that the module is executing a self test, and the Fail LED is lit. If this is a commanded self test, SYSFAIL* is not asserted. In the case of a soft reset, SYSFAIL* is set. However, all Tektronix/CDS commanders will simultaneously set SYSFAIL INHIBIT. This is done to prevent the resource manager from prematurely reporting the failure of a card.

3) If the self test completes successfully, the SYSFAIL* line is released, and the module enters the VXIbus PASSED state (ready for normal operation). SYSFAIL* will be released within 5 seconds in normal operation.

   If the self test fails, the SYSFAIL* line remains active (or is set active, in the case of a commanded self test or soft reset), and the module makes an internal record of what failure(s) occurred. It then enters the VXIbus Failed state, which allows an error message to be returned to the module's commander.

See the Specifications section of this manual for a description of the default condition of the VX4428 Module after the completion of power-up self test.

Self test can also be run at any time during normal operation by using the T command for the transmitter, and the ST command for the receiver. At the end of a commanded self test, the module is restored to its power-up state.

During a commanded self test:

1) SYSFAIL* is not asserted.

2) The module executes the same self test as in the power-up case with the addition of a complete test of the message RAM.

3) If the self test completes successfully, the module restores itself to its power-up state. If the test fails, the SYSFAIL* line is asserted.

SYSFAIL* Operation

SYSFAIL* becomes active during power-up, hard or soft reset, or if the module loses any of its power voltages. When the card cage Resource Manager detects SYSFAIL* set, it will attempt to inhibit the line. This will cause the VX4428 Module to deactivate SYSFAIL* in all cases except when +5 volt power is lost.

Section 4
Programming Examples

This section contains example programs which demonstrate how the various programmable features of the VX4428 are used. The examples are written in both BASIC and C.

Definition of Communication Functions

Both the BASIC and C versions use functions for communication which are not tied to any particular hardware interface. The following list gives each of the functions used and a description of the usage. When using these programs, the functions should be replaced with the corresponding functions for the communication interface being used.

Language	Function
C	void WrtTX(char *OutBuf); void WrtRX(char *OutBuf);
BASIC	WrtTX(OutBuf$) WrtRX(OutBuf$)

These functions write the contents of OutBuf to the VX4488 Transmitter or Receiver. The OutBuf contains ASCII characters with no binary content. The buffer used for the C function must be a null-terminated character string buffer.

C	void WrtTXBin(unsigned char *OutBuf, unsigned int StrLen); void WrtRXBin(unsigned char *OutBuf, unsigned int StrLen);
BASIC	WrtTXBin(OutBuf$, StrLen%) WrtRXBin(OutBuf$, StrLen%)

This function writes the number of bytes specified by StrLen from the contents of OutBuf to the VX4428 Transmitter or Receiver. The OutBuf contains ASCII or binary characters.

C	void RedTX(char *InBuf, unsigned int StrLen); void RedRX(char *InBuf, unsigned int StrLen);
BASIC	RedTX(InBuf$) RedRX(InBuf$)

This function reads from the VX4428 Transmitter or Receiver into the InBuf. The InBuf used for the BASIC function must have the number of bytes expected allocated prior to using this function (use the SPACE$ BASIC function). The C function must have the number of bytes expected specified in the StrLen parameter.

C
```
void RedTXBin(unsigned char *InBuf,
              unsigned int StrLen);
void RedRXBin(unsigned char *InBuf,
              unsigned int StrLen);
```
BASIC
```
RedTXBin(InBuf$, StrLen%)
RedRXBin(InBuf$, StrLen%)
```

This function reads the number of characters specified by StrLen, from the VX4428 Transmitter or Receiver into the InBuf. The InBuf used for the BASIC function must have the number of bytes expected allocated prior to using this function (use the SPACE$ BASIC function).

C
```
void TmDelay(unsigned int MsDelay);
```
BASIC
```
TmDelay(MsDelay%);
```

This function provides a programmable delay timer. The MsDelay variable provides the delay value in milliseconds.

Data Sent and Received

The data sent and received to/from the VX4428 is represented as follows:

1. Binary data is indicated by brackets ([ ]) surrounding a value. The value is indicated using two hex characters for the binary value.

2. Any ASCII carriage return character sent or received is indicated by the <CR> symbol.

3. Any ASCII line feed character sent or received is indicated by the <LF> symbol.

4. Any other character shown is an ASCII character.

5. The write direction is data written TO the VX4428.

6. The read direction is data read back FROM the VX4428.

Programming Examples

C Examples

The C examples assume that the programmer has defined all of the system include files needed by the program. The programmer also needs to include the minimum variable definitions shown below:

```
unsigned char WrtStr[255];   /*Write string buffer. This string buffer will handler both
                             binary and ASCII string storage during write operations
                             to the VX4428.*/

unsigned char RedStr[255];   /*Read string buffer. This string buffer will handler both
                             binary and ASCII string storage during read operations
                             from the VX4428.*/
```

BASIC Examples

The BASIC examples assume that programmer has included all necessary modules needed by the program for both communication and program execution. The programmer also needs to include the minimum variable setups shown below.

```
WrtStr$ = SPACE$(255)   'This reserves space for the write string buffer. This
                        string buffer will handler both binary and ASCII string
                        storage.

RedStr$ = SPACE$(255)   'This reserves space for the read string buffer. This
                        string buffer will handler both binary and ASCII string
                        storage.
```

Example 1: Transmitter Trigger I/O

This program demonstrates the use of the Transmitter Trigger I/O to start transmission. It is assumed that VXIbus TTL trigger lines 0 through 3 are not used by any other card.

In this program, channel 1 will trigger channel 2, channel 2 will trigger channel 3, channel 3 will trigger channel 4, and channel 4 will retrigger channel 1. Channel 1 will be stopped and preset for external triggers as soon as channel 3 starts transmission. Each channel will transmit two words, 8.190 seconds apart. The second word transmitted by each channel will trigger the following channel. All channels will stop after transmitting the second word.

Data Sent and Received During Example 1

Direction	Data
Write	1S40R0A8L[F0][FF][00][80]
Write	[98][01][33][07]
Write	[98][01][33][07]
Write	[F0][FF][00][80]
Write	[00][00][10][80]
Write	[98][01][33][07]
Write	[98][01][33][07]
Write	[00][00][80][80]
Write	2S40R0A8L[F0][FF][00][80]
Write	[98][01][33][07]
Write	[98][01][33][07]
Write	[F0][FF][00][80]
Write	[00][00][10][80]
Write	[98][01][33][07]
Write	[98][01][33][07]
Write	[00][00][80][80]
Write	3S40R0A8L[F0][FF][00][80]
Write	[98][01][33][07]
Write	[98][01][33][07]
Write	[F0][FF][00][80]
Write	[00][00][10][80]
Write	[98][01][33][07]
Write	[98][01][33][07]
Write	[00][00][80][80]
Write	4S40R0A8L[F0][FF][00][80]
Write	[98][01][33][07]
Write	[98][01][33][07]
Write	[F0][FF][00][80]
Write	[00][00][10][80]
Write	[98][01][33][07]
Write	[98][01][33][07]
Write	[00][00][80][80]

Write	180F103X
Write	281F200X
Write	382F301X
Write	448F402X
Write	2P3P4P
Write	1B3S
Read	00000<CR><LF>
.	The preceding read is continued until the value
.	returned is equal to "00003".
.	
Read	00003<CR><LF>
Write	1Q1P

Example 1: BASIC

```
'Defines a header string with the maximum time delay of 4.095 seconds.
HDR1$ = CHR$(240) + CHR$(255) + CHR$(0) + CHR$(128)

'Defines a header with the minimum time delay (5 milliseconds) and
'enables the trigger output for the frame
HDR2$ = CHR$(0) + CHR$(0) + CHR$(16) + CHR$(128)

'Defines a header with the stop bit set
SHEADER$ = CHR$(0) + CHR$(0) + CHR$(128) + CHR$(128)

'Builds a ARINC data word
DTA$ = CHR$(152) + CHR$(1) + CHR$(51) + CHR$(7)

'Builds a complete Header/Data string for the VX4428 Transmitter.
'The string consists of a frame with two data words followed by an
'empty frame, followed by a frame identical to the first frame expect
'for the trigger output bit being set, followed by a stop header.
'Note that the empty second frame will still cause a 4.095 second
'delay before the third frame will be transmitted.
DTAWRT$ = HDR1$ + DTA$ + DTA$ +
          HDR1$ +
          HDR2$ + DTA$ + DTA$ +
          SHEADER$
```

```
'Load each channel with the Header/Data string and setup data.
FOR CHANNEL = 1 TO 4

    'Set up the channel defined the the CHANNEL variable.
    'STR$(CHANNEL) + "S" - Select the active channel.
    '"40R" -  set the active channel's transmitter to the fast bit rate
    '             (100Kbps);.
    '"0A" - set the active channel's load address to 0.
    '"8L" - set the active channel to load 8 Header/Data words
    '        into transmission memory.
    WrtStr$ = STR$(CHANNEL) + "S40R0A8L" + DTAWRT$

    'Transfer the command string to the VX4428 Transmitter.
    CALL WrtTXBin(WrtStr$,LEN(WrtStr$))

NEXT CHANNEL

'Set the channel 1 trigger I/O as follows:
'Trigger Output = VXIbus TTL Trigger Line 0
'Trigger Input  = VXIbus TTL Trigger Line 3
WrtStr$ = "180F103X"
CALL WrtTX(WrtStr$)

'Set the channel 2 trigger I/O as follows:
'Trigger Output = VXIbus TTL Trigger Line 1
'Trigger Input  = VXIbus TTL Trigger Line 0
WrtStr$ = "281F200X"
CALL WrtTX(WrtStr$)

'Set the channel 3 trigger I/O as follows:
'Trigger Output = VXIbus TTL Trigger Line 2
'Trigger Input  = VXIbus TTL Trigger Line 1
WrtStr$ = "382F301X"
CALL WrtTX(WrtStr$)

'Set the channel 4 trigger I/O as follows:
'Trigger Output = VXIbus TTL Trigger Line 3
'Trigger Input  = VXIbus TTL Trigger Line 2
WrtStr$ = "448F402X"
CALL WrtTX(WrtStr$)

'Preset channels 2, 3, and 4 for external trigger input transmission
'start.
WrtStr$ = "2P3P4P"
CALL WrtTX(WrtStr$)

'Start transmission on channel 1 and make channel 3 the active channel.
WrtStr$ = "1B3S"
CALL WrtTX(WrtStr$)
```

```
'Define the number of characters expected back from the Transmitter.
'Note that the string length includes the <CR><LF> returned as part of
'the current transmission address.
RedStr$ = SPACE$(7)

'Read an ASCII string from the Transmitter. This will contain the
'current transmission address for the currently active channel.
'  NOTE : Until the transmitter receives an external trigger input,
'         the transmission address will remain at the next location
'         in memory to be downloaded to the FIFO memory.  In the case
'         of this example, the transmission address will remain at
'         00003.
CALL RedTX(RedStr$)

'Loop until the transmission address for channel 3 changes from
'address 00003.
WHILE(RedStr$ = "00003") : CALL RedTX(RedStr$) : WEND

'Preset channel 1 for external trigger inputs.
WrtStr$ = "1Q1P"
CALL WrtTX(WrtStr$)


'End of the example program 1 in BASIC.
END
```

Example 1: C

```
unsigned char channel;

void main(void)
    {

    /*Load each channel with data.
    for(channel = 1; channel < = 4; channel + +)
        {
        sprintf(WrtStr,
                "%dS"       /*Set the active channel '%dS'; Set the bit rate
                "40R"       to 100Kbps '40R'; Set the data load address to 0
                "0A"        '0A'; Load 8 words of data/control information
                "8L"        '8L'.*/
                "%c%c%c%c"
                "%c%c%c%c"
                "%c%c%c%c"
                "%c%c%c%c"
                "%c%c%c%c"
                "%c%c%c%c"
                "%c%c%c%c"
```

```
                "%c%c%c%c",
                    channel,

                    0xF0,0xFF,0x00,0x80,  /*Defines a header string with the maximum
                                            time delay of 4.095 seconds.*/

                    0x98,0x01,0x33,0x07,  /*Load two ARINC data words in the first
                                            frame.*/
                    0x98,0x01,0x33,0x07,

                    0xF0,0xFF,0x00,0x80,  /*Defines a header string with the maximum
                                            time delay of 4.095 seconds.  Note that this
                                            frame contains no data words to transmit.*/

                    0x00,0x00,0x10,0x80,  /*Defines a header with the minimum time
                                            delay (5 milliseconds) and enables the
                                            trigger output for the frame.*/

                    0x98,0x01,0x33,0x07,  /*Load two ARINC data words in the third
                                            frame.*/
                    0x98,0x01,0x33,0x07,

                    0x00,0x00,0x80,0x80);     /*Define a header with the stop bit set
                                                as the last frame.*/

    WrtTXBin(WrtStr,50);
    }


WrtTX("180F103X");  /*Set the channel 1 trigger I/O as follows:
                    Trigger Output = VXIbus TTL Trigger Line 0
                    Trigger Input  = VXIbus TTL Trigger Line 3*/

WrtTX("281F200X");  /*Set the channel 2 trigger I/O as follows:
                    Trigger Output = VXIbus TTL Trigger Line 1
                    Trigger Input  = VXIbus TTL Trigger Line 0*/

WrtTX("382F301X");  /*Set the channel 3 trigger I/O as follows:
                    Trigger Output = VXIbus TTL Trigger Line 2
                    Trigger Input  = VXIbus TTL Trigger Line 1*/

WrtTX("448F402X");  /*Set the channel 4 trigger I/O as follows:
                    Trigger Output = VXIbus TTL Trigger Line 3
                    Trigger Input  = VXIbus TTL Trigger Line 2*/

WrtTX("2P3P4P");    /*Preset channels 2, 3, and 4 for external trigger input transmission
                    start.*/
```

```
WrtTX("1B3S");          /*Start transmission on channel 1 and make channel 3 the active
                        channel.*/

do {                    /*Loop until the transmission address for channel 3 changes from
                        address 00003.*/

    RedRX(RedStr$,7);       /*Read an ASCII string from the Transmitter. This will contain
                            the current transmission address for the currently active
                            channel. NOTE : Until the transmitter receives an external
                            trigger input, the transmission address will remain at the next
                            location in memory to be downloaded to the FIFO memory. In
                            the case of this example, the transmission address wil remain
                            at 00003. Note that the string length includes the
                            <CR><LF> returned as part of the current transmission
                            address.*/

} while(!(strncmp("00003",RedStr$,5)));

WrtTX("1Q1P");          /*Preset channel 1 for external trigger inputs.*/


}                       /*End of the example program 1 in C.*/
```

Example 2: Receiver Monitor Mode

This sample program uses the Receivers Monitor mode without time-stamp/error storage to capture data from the ARINC bus, and display the hex value of each byte of 6 words of received ARINC data. The data transmitted over the ARINC bus is assumed to have the following values and data transmission sequence (word 1 is transmitted first followed by word 2, ..., etc.).

ARINC Bit Position	ARINC Word 1	2	3	4	5	6	7	8
1	1	0	0	0	0	1	0	0
2	0	1	1	0	0	0	0	0
3	0	0	0	0	0	0	0	1
4	1	0	1	1	1	1	0	0
5	1	0	0	0	1	0	1	0
6	0	0	1	0	0	0	0	1
7	0	0	0	1	1	1	0	1
8	0	0	1	1	0	0	0	0
9	1	0	0	0	0	0	0	0
10	0	1	0	0	0	0	0	0
11	0	0	1	0	0	0	0	0
12	0	0	0	1	0	0	0	0
13	0	0	0	0	1	0	0	0
14	0	0	0	0	0	1	0	0
15	0	0	0	0	0	0	1	0
16	0	0	0	0	0	0	0	1
17	1	0	1	1	0	0	0	1
18	1	0	0	1	0	0	0	1
19	0	1	1	1	0	0	1	1
20	0	1	0	1	0	0	1	1
21	1	0	1	0	1	0	1	1
22	1	0	0	0	1	0	1	1
23	0	1	1	0	1	0	0	1
24	0	1	0	0	1	0	0	1
25	1	0	0	0	0	1	1	0
26	1	1	0	0	0	0	1	0
27	1	1	1	0	0	0	0	1
28	0	1	1	1	0	0	0	1
29	0	0	1	1	1	0	0	1
30	0	0	0	1	1	1	0	1
31	0	0	0	0	1	1	1	0
32	0	0	1	0	0	0	0	1

Data Sent and Received During Example 2

Direction	Data	
Write	RS1RC1SC0MM0DS0TD0IN1BR1RE	
Write	2SD	
Read	[XX][XX]	This sequence repeats until the received stored word count is greater than or equal to 6.
	.	
	.	
Write	2SD	
Read	[06][00]	
Read	[98][01][33][07]	
Read	[40][02][CC][0E]	
Read	[55][04][55][9C]	
Read	[13][08][0F][38]	
Read	[1A][10][F0][70]	
Read	[92][20][00][61]	

Example 2: BASIC

```
'This command resets the module, connects the channel 1 receiver to the main input
'connector, sets channel 1 to Monitor mode without time-stamp/error storage, no
'<CR><LF> data termination, interrupts disabled, selects the fast bit rate, and enables the
'channel 1 receiver. It is assumed that data transmission starts on the ARINC bus after the
'receivers are enabled.

WrtStr$ = "RS1RC1SC0MM0DS0TD0IN1BR1RE"
CALL WrtRX(WrtStr$)

'Use the 2SD command to determine the number of words currently
'stored.
WrtStr$ = "2SD"
CALL WrtRX(WrtStr$)

'Read the two bytes indicating the number of words stored and
'convert to an integer.
CALL RedRXBin(RedStr$,2)
WrdsStrd = ASC(MID$(RedStr$,1,1)) + (256*ASC(MID$(RedStr$,2,1)))

'Loop until the number of words stored equals or exceeds 6.
WHILE(WrdsStrd < 6 )
      CALL WrtRX(WrtStr$)
      CALL RedRXBin(RedStr$,2)
      WrdsStrd = ASC(MID$(RedStr$,1,1)) + (256*ASC(MID$(RedStr$,2,1)))
WEND
```

```
'Read 6 ARINC words from the Receiver, convert each byte of the
'received data to a hex string, and print each word.
RedStr$ = SPACE$(24)
CALL RedRXBin(RedStr$,24)
FOR I = 0 TO 5
      RECDTA$ = ""
      FOR J = 1 TO 4
            BYT$ = HEX$(ASC(MID$(RedStr$,((I*4)+J),1)))
            IF LEN(BYT$) = 1 THEN BYT$ = "0" + BYT$
            RECDTA$ = RECDTA$ + BYT$ + SPACE$(1)
      NEXT J
      PRINT RECDTA$
NEXT I

'End of the example program 2 in BASIC.
END
```

Example 2: C

```
void main(void)
      {

      unsigned int WrdsStrd;  /*Variable holding the number of words
                                    currently stored.*/

      /*This command resets the module, connects the channel 1 receiver to the main input
      connector, sets channel 1 to Monitor mode without time-stamp/error storage, no
      <CR><LF> data termination, interrupts disabled, selects the fast bit rate, and enables the
      channel 1 receiver.  It is assumed that data transmission starts on the ARINC bus after the
      receivers are enabled.*/
      WrtRX("RS1RC1SC0MM0DS0TD0IN1BR1RE");

      /*Wait until 6 or more words are stored on the receiver.*/
      do    {

            /*Use the 2SD command to determine the number of words currently stored.*/
            WrtRX("2SD");

            /*Read the two bytes indicating the number of words stored and convert to an
            integer.*/
            RedRXBin(RedStr,2)
            WrdsStrd = RedStr[0] + (256 * RedStr[1]);

            }while(WrdsStrd < 6);

      /*Read 6 ARINC words from the Receiver, convert each byte of the received data to a hex
      string, and print each word.*/
```

```
WrtRX("16SD");
RedRXBin(RedStr,24);
printf("%2X %2X %2X %2X/n"
        "%2X %2X %2X %2X/n"
        "%2X %2X %2X %2X/n"
        "%2X %2X %2X %2X/n"
        "%2X %2X %2X %2X/n",
        RedStr[0], RedStr[1], RedStr[2], RedStr[3],
        RedStr[4], RedStr[5], RedStr[6], RedStr[7],
        RedStr[8], RedStr[9], RedStr[10],RedStr[11],
        RedStr[12],RedStr[13],RedStr[14],RedStr[15],
        RedStr[16],RedStr[17],RedStr[18],RedStr[19],
        RedStr[20],RedStr[21],RedStr[22],RedStr[23]);

}
/*End of the example program 2 in C.*/
```

Example 3: Receiver Limit-Check Mode

This sample program uses the VX4428 Receiver's Limit-check Mode without time-stamp/error storage to capture data on the ARINC bus and display the hex value of the stored data. The data transmitted over the ARINC bus is assumed to have the following values and data transmission sequence (word 1 is transmitted first, followed by word 2, ..., etc.).

ARINC Bit Position	ARINC Word 1	2	3	4	5	6	7	8	9	10	11	12
1	0	1	0	0	0	0	0	0	0	1	0	0
2	0	0	0	1	0	1	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0	0	0	0	0
4	1	1	1	0	1	1	1	1	1	1	1	0
5	0	1	0	0	0	0	0	1	0	0	0	1
6	0	0	0	0	0	1	0	0	0	0	0	0
7	1	0	1	0	1	0	1	1	1	1	1	0
8	1	0	1	0	1	1	1	0	1	0	1	0
9	0	0	0	0	0	0	0	0	0	0	0	0
10	0	1	0	1	0	1	0	1	0	1	0	1
11	0	0	0	0	0	0	0	0	0	0	0	0
12	0	1	0	1	0	1	0	1	0	1	0	1
13	0	0	0	0	0	0	0	0	0	0	0	0
14	0	1	0	1	0	1	0	1	0	1	0	1
15	0	0	0	0	0	0	0	0	0	0	0	0
16	0	1	0	1	0	1	0	1	0	1	0	1
17	0	0	0	0	0	0	0	0	0	0	0	0
18	0	1	0	1	0	1	0	1	0	1	0	1
19	0	0	0	0	0	0	0	0	0	0	0	0
20	0	1	0	1	0	1	0	1	0	1	0	1
21	0	0	0	0	0	0	0	0	0	0	0	0
22	0	1	0	1	1	1	0	1	1	1	0	1
23	0	0	1	0	0	0	0	0	0	0	1	0
24	1	1	0	1	0	1	0	1	0	1	0	1
25	0	0	0	0	0	0	0	0	0	0	0	0
26	1	1	1	1	1	1	1	1	1	1	1	1
27	1	0	1	0	1	0	1	0	1	0	1	0
28	1	1	1	1	1	1	1	1	1	1	1	1
29	1	0	1	0	1	0	1	0	1	0	1	0
30	1	1	1	1	1	1	1	1	1	1	1	1
31	1	0	1	0	1	0	1	0	1	0	1	0
32	1	1	1	1	1	0	0	1	1	1	1	1

Data Sent and Received During Example 2

Direction	Data	
Write	RS2RC2SC2MM0DS0TD0IN1BR	
Write	2PR1PT	
Write	SL[13][0]	
Write	1LP[0][0][7E]	
Write	2RE	
Write	EX	
Read	[00]<CR><LF>	This sequence repeats until the status byte indicates that the preset conditions have been met.
	.	
	.	
	.	
Write	EX	
Read	[04]<CR><LF>	
Write	2SD	
Read	[04][00]	
Read	[13][00][40][FE]	
Read	[13][00][20][FE]	
Read	[13][00][00][7E]	
Read	[13][00][20][FE]	
Read	[13][00][40][FE]	

Example 3: BASIC

```
'This command resets the module, connects the channel 2 receiver
'to the input connector, sets channel 2 to Limit-check mode
'without time-stamp/error storage, no <CR><LF> data termination,
'disables interrupts, and selects the fast bit rate. It is assumed
'that data transmission starts on the ARINC bus after the
'receivers are enabled.
WrtStr$ = "RS2RC2SC2MM0DS0TD0IN1BR"
CALL WrtRX(WrtStr$)

'Set the channel to capture 2 words before and 1 word after the
'trigger event.
WrtStr$ = "2PR1PT"
CALL WrtRX(WrtStr$)

'Set the label to capture to octal 023, capture based on the label
'only.
WrtStr$ = "SL" + CHR$(19) + CHR$(0)
```

```
CALL WrtRXBin(WrtStr$,4)

'Set the trigger event to occur when the second and third stored
'bytes of the received ARINC word are equal to zero and the fourth
'byte of the received ARINC word is equal to decimal 126.
WrtStr$ = "1LP" + CHR$(0) + CHR$(0) + CHR$(126)
CALL WrtRXBin(WrtStr$,6)

'Enable the receiver.
WrtStr$ = "2RE"
CALL WrtRX(WrtStr$)

'Write the EX (Examine Status) command to the receiver in order to
'determine when the channel has triggered and completed data
'reception.
WrtStr$ = "EX"
CALL WrtRX(WrtStr$)

'Read the status byte from the receiver.  Note that the read includes
'the <CR><LF> termination characters.
CALL RedRXBin(RedStr$,3)

'Continue examining the status byte until the channel 2 status bit
'goes active indicating the completion of the data storage for the
'limit check mode.
WHILE(ASC(MID$(RedStr$,1,1) AND 4) < > 4)
      CALL WrtRX(WrtStr$)
      CALL RedRXBin(RedStr$,3)
WEND

'Use the 2SD command to determine the number of words store.  This
'can be used to ensure the preset number of words stored.
WrtStr$ = "2SD"
CALL WrtRX(WrtStr$)

'Read the two bytes indicating the number of words stored and
'convert to an integer.
CALL RedRXBin(RedStr$,2)
WrdsStrd = ASC(MID$(RedStr$,1,1)) + (256*ASC(MID$(RedStr$,2,1)))


FOR I = 0 TO (WrdsStrd - 1)
      RedRXBin(RedStr$,4)
      RECDTA$ = ""
      FOR J = 1 TO 4
            BYT$ = HEX$(ASC(MID$(RedStr$,J,1)))
            IF LEN(BYT$) = 1 THEN BYT$ = "0" + BYT$
            RECDTA$ = RECDTA$ + BYT$ + SPACE$(1)
      NEXT J
```

```
        PRINT RECDTA$
    NEXT I

    'End of the example program 3 in BASIC.
    END
```

Example 3: C

```
void main(void)
    {

    unsigned int WrdsStrd;  /*Variable holding the number of words currently stored.*/

    unsigned int i;         /*Loop counter variable.*/

    /*This command resets the module, connects the channel 2 receiver to the input connector,
    sets channel 2 to Limit-check mode without time-stamp/error storage, no <CR><LF> data
    termination, disables interrupts, and selects the fast bit rate.  It is assumed that data
    transmission starts on the ARINC bus after the receivers are enabled.*/
    WrtRX("RS2RC2SC2MM0DS0TD0IN1BR");

    /*Set the channel to capture 2 words before and 1 word after the trigger event.*/
    WrtRX("2PR1PT");

    /*Set the label to capture to octal 023, capture based on the label only.*/
    sprintf(WrtStr,"SL%c%c",19,0);
    WrtRXBin(WrtStr,4);

    /*Set the trigger event to occur when the second and third stored bytes of the received
    ARINC word are equal to zero and the fourth byte of the received ARINC word is equal to
    decimal 126.*/
    sprintf(WrtStr,"1LP%c%c%c",0,0,126);
    WrtRXBin(WrtStr,6);

    /*Enable the receiver.*/
    WrtRX$("2RE");

    /*Continue examining the status byte until the channel 2 status bit goes active indicating the
    completion of the data storage for the limit check mode.*/
    do  {

        /*Write the EX (Examine Status) command to the receiver in order to determine when
        the channel has triggered and completed data reception.*/
        WrtRX("EX");

        /*Read the status byte from the receiver.  Note that the read includes the <CR><LF>
        termination characters.*/
```

```
        RedRXBin(RedStr,3);


        }while((RedStr[0] & 0x04) != 0x04);

/*Use the 2SD command to determine the number of words store.  This can be used to
ensure the preset number of words stored.*/
WrtRX("2SD");

/*Read the two bytes indicating the number of words stored and convert to an integer.*/
RedRXBin(RedStr,2)
WrdsStrd = RedStr[0] + (256 * RedStr[1]);

for(i = 0; i < WrdsStrd; i++)
        {
        RedRXBin(RedStr,4);
        printf("%2X %2X %2X %2X\n",
                RedStr[0],RedStr[1],RedStr[2],RedStr[3]);
        }

}
/*End of the example program 3 in C.*/
```

Example 4: Receiver and Transmitter Loopback Self-Test

This sample program uses the VX4428's self-test data path to perform a test of the transmitter and receiver. Each transmitter channel will transmit 31 ARINC words to the receiver and then stop transmission. The ARINC data sent and received will contain a walking one's data pattern as shown below.

ARINC Bit	ARINC Word																															
										1	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	2	2	3	3
Position	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1
1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
3	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
5	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
18	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
19	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
20	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
21	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
23	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
26	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
27	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
28	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
29	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
30	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
31	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
32	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Data Sent and Received During Example 2

Direction	Data	Source/Destination
Write	K1S40R2S40R3S40R4S40R	Transmitter
Write	RS	Receiver
Write	1SC0MM0DS0TD1BR	Receiver
Write	2SC0MM0DS0TD1BR	Receiver
Write	3SC0MM0DS0TD1BR	Receiver
Write	4SC0MM0DS0TD1BR	Receiver
Write	1S0A33L	Transmitter
Write	[00][08][00][80]	Transmitter
Write	[01][00][00][00]	Transmitter
Write	[02][00][00][00]	Transmitter
Write	[04][00][00][00]	Transmitter
Write	[08][00][00][00]	Transmitter
Write	[10][00][00][00]	Transmitter
Write	[20][00][00][00]	Transmitter
Write	[40][00][00][00]	Transmitter
Write	[80][00][00][00]	Transmitter
Write	[00][01][00][00]	Transmitter
Write	[00][02][00][00]	Transmitter
Write	[00][04][00][00]	Transmitter
Write	[00][08][00][00]	Transmitter
Write	[00][10][00][00]	Transmitter
Write	[00][20][00][00]	Transmitter
Write	[00][40][00][00]	Transmitter
Write	[00][80][00][00]	Transmitter
Write	[00][00][01][00]	Transmitter
Write	[00][00][02][00]	Transmitter
Write	[00][00][04][00]	Transmitter
Write	[00][00][08][00]	Transmitter
Write	[00][00][10][00]	Transmitter
Write	[00][00][20][00]	Transmitter
Write	[00][00][40][00]	Transmitter
Write	[00][00][80][00]	Transmitter
Write	[00][00][00][01]	Transmitter
Write	[00][00][00][02]	Transmitter
Write	[00][00][00][04]	Transmitter
Write	[00][00][00][08]	Transmitter
Write	[00][00][00][10]	Transmitter
Write	[00][00][00][20]	Transmitter
Write	[00][00][00][40]	Transmitter

Write	[00][00][00][80]	Transmitter
Write	2S0A33L	Transmitter
Write	[00][08][00][80]	Transmitter
Write	[01][00][00][00]	Transmitter
Write	[02][00][00][00]	Transmitter
Write	[04][00][00][00]	Transmitter
Write	[08][00][00][00]	Transmitter
Write	[10][00][00][00]	Transmitter
Write	[20][00][00][00]	Transmitter
Write	[40][00][00][00]	Transmitter
Write	[80][00][00][00]	Transmitter
Write	[00][01][00][00]	Transmitter
Write	[00][02][00][00]	Transmitter
Write	[00][04][00][00]	Transmitter
Write	[00][08][00][00]	Transmitter
Write	[00][10][00][00]	Transmitter
Write	[00][20][00][00]	Transmitter
Write	[00][40][00][00]	Transmitter
Write	[00][80][00][00]	Transmitter
Write	[00][00][01][00]	Transmitter
Write	[00][00][02][00]	Transmitter
Write	[00][00][04][00]	Transmitter
Write	[00][00][08][00]	Transmitter
Write	[00][00][10][00]	Transmitter
Write	[00][00][20][00]	Transmitter
Write	[00][00][40][00]	Transmitter
Write	[00][00][80][00]	Transmitter
Write	[00][00][00][01]	Transmitter
Write	[00][00][00][02]	Transmitter
Write	[00][00][00][04]	Transmitter
Write	[00][00][00][08]	Transmitter
Write	[00][00][00][10]	Transmitter
Write	[00][00][00][20]	Transmitter
Write	[00][00][00][40]	Transmitter
Write	[00][00][00][80]	Transmitter
Write	3S0A33L	Transmitter
Write	[00][08][00][80]	Transmitter
Write	[01][00][00][00]	Transmitter
Write	[02][00][00][00]	Transmitter
Write	[04][00][00][00]	Transmitter
Write	[08][00][00][00]	Transmitter

Write	[10][00][00][00]	Transmitter
Write	[20][00][00][00]	Transmitter
Write	[40][00][00][00]	Transmitter
Write	[80][00][00][00]	Transmitter
Write	[00][01][00][00]	Transmitter
Write	[00][02][00][00]	Transmitter
Write	[00][04][00][00]	Transmitter
Write	[00][08][00][00]	Transmitter
Write	[00][10][00][00]	Transmitter
Write	[00][20][00][00]	Transmitter
Write	[00][40][00][00]	Transmitter
Write	[00][80][00][00]	Transmitter
Write	[00][00][01][00]	Transmitter
Write	[00][00][02][00]	Transmitter
Write	[00][00][04][00]	Transmitter
Write	[00][00][08][00]	Transmitter
Write	[00][00][10][00]	Transmitter
Write	[00][00][20][00]	Transmitter
Write	[00][00][40][00]	Transmitter
Write	[00][00][80][00]	Transmitter
Write	[00][00][00][01]	Transmitter
Write	[00][00][00][02]	Transmitter
Write	[00][00][00][04]	Transmitter
Write	[00][00][00][08]	Transmitter
Write	[00][00][00][10]	Transmitter
Write	[00][00][00][20]	Transmitter
Write	[00][00][00][40]	Transmitter
Write	[00][00][00][80]	Transmitter
Write	4S0A33L	Transmitter
Write	[00][08][00][80]	Transmitter
Write	[01][00][00][00]	Transmitter
Write	[02][00][00][00]	Transmitter
Write	[04][00][00][00]	Transmitter
Write	[08][00][00][00]	Transmitter
Write	[10][00][00][00]	Transmitter
Write	[20][00][00][00]	Transmitter
Write	[40][00][00][00]	Transmitter
Write	[80][00][00][00]	Transmitter
Write	[00][01][00][00]	Transmitter
Write	[00][02][00][00]	Transmitter
Write	[00][04][00][00]	Transmitter
Write	[00][08][00][00]	Transmitter

Write	[00][10][00][00]	Transmitter
Write	[00][20][00][00]	Transmitter
Write	[00][40][00][00]	Transmitter
Write	[00][80][00][00]	Transmitter
Write	[00][00][01][00]	Transmitter
Write	[00][00][02][00]	Transmitter
Write	[00][00][04][00]	Transmitter
Write	[00][00][08][00]	Transmitter
Write	[00][00][10][00]	Transmitter
Write	[00][00][20][00]	Transmitter
Write	[00][00][40][00]	Transmitter
Write	[00][00][80][00]	Transmitter
Write	[00][00][00][01]	Transmitter
Write	[00][00][00][02]	Transmitter
Write	[00][00][00][04]	Transmitter
Write	[00][00][00][08]	Transmitter
Write	[00][00][00][10]	Transmitter
Write	[00][00][00][20]	Transmitter
Write	[00][00][00][40]	Transmitter
Write	[00][00][00][80]	Transmitter
Write	RE	Receiver
Write	B	Transmitter
Write	1SC	Receiver
Read	[01][00][00][00]	Receiver
Read	[02][00][00][00]	Receiver
Read	[04][00][00][00]	Receiver
Read	[08][00][00][00]	Receiver
Read	[10][00][00][00]	Receiver
Read	[20][00][00][00]	Receiver
Read	[40][00][00][00]	Receiver
Read	[80][00][00][00]	Receiver
Read	[00][01][00][00]	Receiver
Read	[00][02][00][00]	Receiver
Read	[00][04][00][00]	Receiver
Read	[00][08][00][00]	Receiver
Read	[00][10][00][00]	Receiver
Read	[00][20][00][00]	Receiver
Read	[00][40][00][00]	Receiver
Read	[00][80][00][00]	Receiver
Read	[00][00][01][00]	Receiver

Read	[00][00][02][00]	Receiver
Read	[00][00][04][00]	Receiver
Read	[00][00][08][00]	Receiver
Read	[00][00][10][00]	Receiver
Read	[00][00][20][00]	Receiver
Read	[00][00][40][00]	Receiver
Read	[00][00][80][00]	Receiver
Read	[00][00][00][01]	Receiver
Read	[00][00][00][02]	Receiver
Read	[00][00][00][04]	Receiver
Read	[00][00][00][08]	Receiver
Read	[00][00][00][10]	Receiver
Read	[00][00][00][20]	Receiver
Read	[00][00][00][40]	Receiver
Write	2SC	Receiver
Read	[01][00][00][00]	Receiver
Read	[02][00][00][00]	Receiver
Read	[04][00][00][00]	Receiver
Read	[08][00][00][00]	Receiver
Read	[10][00][00][00]	Receiver
Read	[20][00][00][00]	Receiver
Read	[40][00][00][00]	Receiver
Read	[80][00][00][00]	Receiver
Read	[00][01][00][00]	Receiver
Read	[00][02][00][00]	Receiver
Read	[00][04][00][00]	Receiver
Read	[00][08][00][00]	Receiver
Read	[00][10][00][00]	Receiver
Read	[00][20][00][00]	Receiver
Read	[00][40][00][00]	Receiver
Read	[00][80][00][00]	Receiver
Read	[00][00][01][00]	Receiver
Read	[00][00][02][00]	Receiver
Read	[00][00][04][00]	Receiver
Read	[00][00][08][00]	Receiver
Read	[00][00][10][00]	Receiver
Read	[00][00][20][00]	Receiver
Read	[00][00][40][00]	Receiver
Read	[00][00][80][00]	Receiver
Read	[00][00][00][01]	Receiver
Read	[00][00][00][02]	Receiver
Read	[00][00][00][04]	Receiver
Read	[00][00][00][08]	Receiver

Read	[00][00][00][10]	Receiver
Read	[00][00][00][20]	Receiver
Read	[00][00][00][40]	Receiver
Write	3SC	Receiver
Read	[01][00][00][00]	Receiver
Read	[02][00][00][00]	Receiver
Read	[04][00][00][00]	Receiver
Read	[08][00][00][00]	Receiver
Read	[10][00][00][00]	Receiver
Read	[20][00][00][00]	Receiver
Read	[40][00][00][00]	Receiver
Read	[80][00][00][00]	Receiver
Read	[00][01][00][00]	Receiver
Read	[00][02][00][00]	Receiver
Read	[00][04][00][00]	Receiver
Read	[00][08][00][00]	Receiver
Read	[00][10][00][00]	Receiver
Read	[00][20][00][00]	Receiver
Read	[00][40][00][00]	Receiver
Read	[00][80][00][00]	Receiver
Read	[00][00][01][00]	Receiver
Read	[00][00][02][00]	Receiver
Read	[00][00][04][00]	Receiver
Read	[00][00][08][00]	Receiver
Read	[00][00][10][00]	Receiver
Read	[00][00][20][00]	Receiver
Read	[00][00][40][00]	Receiver
Read	[00][00][80][00]	Receiver
Read	[00][00][00][01]	Receiver
Read	[00][00][00][02]	Receiver
Read	[00][00][00][04]	Receiver
Read	[00][00][00][08]	Receiver
Read	[00][00][00][10]	Receiver
Read	[00][00][00][20]	Receiver
Read	[00][00][00][40]	Receiver
Write	4SC	Receiver
Read	[01][00][00][00]	Receiver
Read	[02][00][00][00]	Receiver
Read	[04][00][00][00]	Receiver
Read	[08][00][00][00]	Receiver
Read	[10][00][00][00]	Receiver
Read	[20][00][00][00]	Receiver

Read	[40][00][00][00]	Receiver
Read	[80][00][00][00]	Receiver
Read	[00][01][00][00]	Receiver
Read	[00][02][00][00]	Receiver
Read	[00][04][00][00]	Receiver
Read	[00][08][00][00]	Receiver
Read	[00][10][00][00]	Receiver
Read	[00][20][00][00]	Receiver
Read	[00][40][00][00]	Receiver
Read	[00][80][00][00]	Receiver
Read	[00][00][01][00]	Receiver
Read	[00][00][02][00]	Receiver
Read	[00][00][04][00]	Receiver
Read	[00][00][08][00]	Receiver
Read	[00][00][10][00]	Receiver
Read	[00][00][20][00]	Receiver
Read	[00][00][40][00]	Receiver
Read	[00][00][80][00]	Receiver
Read	[00][00][00][01]	Receiver
Read	[00][00][00][02]	Receiver
Read	[00][00][00][04]	Receiver
Read	[00][00][00][08]	Receiver
Read	[00][00][00][10]	Receiver
Read	[00][00][00][20]	Receiver
Read	[00][00][00][40]	Receiver

Example 4: BASIC

```
'Set up the bit rates on the VX4428 Transmitter to fast bit rate.
WrtStr$ = "K1S40R2S40R3S40R4S40R"
CALL WrtTX(WrtStr$)

'Set up the operating mode for the VX4428 Receiver.
'Monitor Mode; No timestamp; no data termination character;
'fast bitrate.
WrtStr$ = "RS1SCOMMODS0TD1BR2SCOMMODS0TD1BR3SCOMMODS0TD1BR"
WrtStr$ = WrtStr$ + "4SCOMMODS0TD1BR"
CALL WrtTX(WrtStr$)

FOR CurChan = 1 TO 4

    'Load the VX4428 s with a walking ones data pattern.
    'The data pattern consists of header with a frame delay of XX
```

```
        'milliseconds duration, followed by 31 data words, followed by
        'a stop header.
        WrtStr$ = STR$(CurChan) + "S0A33L"
        WrtStr$ = WrtStr$ + CHR$(0) + CHR$(8) + CHR$(0) + CHR$(128)
        WrtTXBin(WrtStr$,11);

        'Write walking ones data to the transmitter.
        FOR II = 0 TO 7

            WrtStr$ = CHR$(2^II) + CHR$(0) + CHR$(0) + CHR$(0)
            WrtTXBin(WrtStr$,4);

        NEXT II

        'Write walking ones data to the transmitter.
        FOR II = 0 TO 7

            WrtStr$ = CHR$(0) + CHR$(2^II) + CHR$(0) + CHR$(0)
            WrtTXBin(WrtStr$,4);

        NEXT II

        'Write walking ones data to the transmitter.
        FOR II = 0 TO 7

            WrtStr$ = CHR$(0) + CHR$(0) + CHR$(2^II) + CHR$(0)
            WrtTXBin(WrtStr$,4);

        NEXT II

        'Write walking ones data to the transmitter.
        FOR II = 0 TO 6

            WrtStr$ = CHR$(2^II) + CHR$(0) + CHR$(0) + CHR$(2^II)
            WrtTXBin(WrtStr$,4);

        NEXT II

        'Load the transmitter with a stop header.
        WrtStr$ = CHR$(0) + CHR$(0) + CHR$(128) + CHR$(128)
        WrtTXBin(WrtStr,4);

    NEXT CurChan

    'Enable all of the Receiver channels.
    WrtStr$ = "RE"
    CALL WrtTX(WrtStr$)

    'Delay while the receivers are enabling.
```

```
TmDelay(100)

'Start Transmission on all of the VX4428 Transmitter channels.
WrtStr$ = "B"
CALL WrtTX(WrtStr$)

'Delay to allow the transmitter to complete transmission.
TmDelay(500)

'Check the data transmitted by all channels.
FOR CurChan = 1 TO 4

    'Set the active receiver channel.
    WrtStr$ = STR$(CurChan) + "SC"
    CALL WrtRX(WrtStr$)

    'Read and compare ARINC words from the Receiver.
    FOR II = 0 TO 7

        'Read 1 word from the Receiver
        CALL RedRX(RedStr$,4);

        'Set up a comparison string containing the correct received
        'data.
        CmpStr$ = CHR$(2^II) + CHR$(0) + CHR$(0) + CHR$(0)

        /*Compare the received data with the expected data.*/
        IF MID$(RedStr$,1,4) < > CmpStr$ THEN

            RECDTA$ = "Error in Channel " + STR$(CurChan)
            RECDTA$ = " Self-Test Data."
            PRINT RECDTA$
            RECDTA$ = "Expected Data = " + HEX$(2^II) + " 00 00 00"
            PRINT RECDTA$
            RECDTA$ = "Received Data = "
            FOR J = 1 TO 4
                BYT$ = HEX$(ASC(MID$(RedStr$,J,1)))
                IF LEN(BYT$) = 1 THEN BYT$ = "0" + BYT$
                RECDTA$ = RECDTA$ + BYT$ + SPACE$(1)
            NEXT J
            PRINT RECDTA$

        END IF
    NEXT II

    'Read and compare ARINC words from the Receiver.
    FOR II = 0 TO 7

        'Read 1 word from the Receiver
```

```
        CALL RedRX(RedStr$,4);

        'Set up a comparison string containing the correct received
        'data.
        CmpStr$ = CHR$(0) + CHR$(2^II) + CHR$(0) + CHR$(0)

        /*Compare the received data with the expected data.*/
        IF MID$(RedStr$,1,4) < > CmpStr$ THEN

            RECDTA$ = "Error in Channel " + STR$(CurChan)
            RECDTA$ = " Self-Test Data."
            PRINT RECDTA$
            RECDTA$ = "Expected Data = 00 " + HEX$(2^II) + " 00 00"
            PRINT RECDTA$
            RECDTA$ = "Received Data = "
            FOR J = 1 TO 4
                BYT$ = HEX$(ASC(MID$(RedStr$,J,1)))
                IF LEN(BYT$) = 1 THEN BYT$ = "0" + BYT$
                RECDTA$ = RECDTA$ + BYT$ + SPACE$(1)
            NEXT J
            PRINT RECDTA$

        END IF
NEXT II

'Read and compare ARINC words from the Receiver.
FOR II = 0 TO 7

        'Read 1 word from the Receiver
        CALL RedRX(RedStr$,4);

        'Set up a comparison string containing the correct received
        'data.
        CmpStr$ = CHR$(0) + CHR$(0) + CHR$(2^II) + CHR$(0)

        /*Compare the received data with the expected data.*/
        IF MID$(RedStr$,1,4) < > CmpStr$ THEN

            RECDTA$ = "Error in Channel " + STR$(CurChan)
            RECDTA$ = " Self-Test Data."
            PRINT RECDTA$
            RECDTA$ = "Expected Data = 00 00 " + HEX$(2^II) + " 00"
            PRINT RECDTA$
            RECDTA$ = "Received Data = "
            FOR J = 1 TO 4
                BYT$ = HEX$(ASC(MID$(RedStr$,J,1)))
                IF LEN(BYT$) = 1 THEN BYT$ = "0" + BYT$
                RECDTA$ = RECDTA$ + BYT$ + SPACE$(1)
            NEXT J
```

```
                PRINT RECDTA$

            END IF
        NEXT II

        'Read and compare ARINC words from the Receiver.
        FOR II = 0 TO 6

            'Read 1 word from the Receiver
            CALL RedRX(RedStr$,4);

            'Set up a comparison string containing the correct received
            'data.
            CmpStr$ = CHR$(0) + CHR$(0) + CHR$(0) + CHR$(2^II)

            /*Compare the received data with the expected data.*/
            IF MID$(RedStr$,1,4) <> CmpStr$ THEN

                RECDTA$ = "Error in Channel " + STR$(CurChan)
                RECDTA$ = " Self-Test Data."
                PRINT RECDTA$
                RECDTA$ = "Expected Data = 00 00 00 " + HEX$(2^II)
                PRINT RECDTA$
                RECDTA$ = "Received Data = "
                FOR J = 1 TO 4
                    BYT$ = HEX$(ASC(MID$(RedStr$,J,1)))
                    IF LEN(BYT$) = 1 THEN BYT$ = "0" + BYT$
                    RECDTA$ = RECDTA$ + BYT$ + SPACE$(1)
                NEXT J
                PRINT RECDTA$

            END IF
        NEXT II

    NEXT CurChan

    'End of the example program 4 in BASIC.
    END
```

Example 4: C

```
void main(void)
    {
    unsigned char CurChan;      /*Current channel variable.*/
    int ii;                     /*Loop counter variable.*/

    /*Set up the bit rates on the VX4428 Transmitter to fast bit rate.*/
```

```
WrtTX("K1S40R2S40R3S40R4S40R");

/*Set up the operating mode for the VX4428 Receiver.
/*Monitor Mode; No timestamp; no data termination character;
  fast bitrate.*/
WrtRX("RS1SCOMMODSOTD1BR"
      "2SCOMMODSOTD1BR"
      "3SCOMMODSOTD1BR"
      "4SCOMMODSOTD1BR");

for(CurChan = 1; CurChan <=4; CurChan++)
      {
      /*Load the VX4428 Transmitters with a walking ones data pattern. The data pattern
      consists of header with a frame delay of XX milliseconds duration, followed by 31 data
      words, followed by a stop header.*/
      sprintf(WrtStr,"%dS0A33L%c%c%c%c",CurChan,0x00,0x08,0x00,0x80);
      WrtTXBin(WrtStr,11);

      /*Write walking ones data to the transmitter.*/
      for(ii=0x01; ii <= 0x80; ii<<1)
            {
            sprintf(WrtStr,"%c%c%c%c",ii,0x00,0x00,0x00);
            WrtTXBin(WrtStr,4);
            }
      /*Write walking ones data to the transmitter.*/
      for(ii=0x01; ii <= 0x80; ii<<1)
            {
            sprintf(WrtStr,"%c%c%c%c",0x00,ii,0x00,0x00);
            WrtTXBin(WrtStr,4);
            }
      /*Write walking ones data to the transmitter.*/
      for(ii=0x01; ii <= 0x80; ii<<1)
            {
            sprintf(WrtStr,"%c%c%c%c",0x00,0x00,ii,0x00);
            WrtTXBin(WrtStr,4);
            }
      /*Write walking ones data to the transmitter.*/
      for(ii=0x01; ii <= 0x40; ii<<1)
            {
            sprintf(WrtStr,"%c%c%c%c",ii,0x00,0x00,ii);
            WrtTXBin(WrtStr,4);
            }
      /*Load the transmitter with a stop header.*/
      sprintf(WrtStr,"%c%c%c%c",0x00,0x00,0x80,0x80);
      WrtTXBin(WrtStr,4);
      }

/*Enable all of the Receiver channels.*/
WrtRX("RE");
```

```
/*Delay while the receivers are enabling.*/
TmDelay(100);

/*Start Transmission on all of the VX4428 Transmitter channels.*/
WrtTX("B");

/*Delay to allow the transmitter to complete transmission.*/
TmDelay(500);

/*Check the data transmitted by all channels*/
for(CurChan = 1; CurChan <= 4; CurChan++)
      {
      /*Set the active receiver channel.*/
      sprintf(holdstr,"%dSC",CurChan);
      WrtRX(holdstr);

      /*Read and compare ARINC words from the Receiver.*/
      for(ii=1; ii <= 0x80; ii<<1)
            {
            /*Read 1 word from the Receiver*/
            RedRX(RedStr,4);

            /*Compare the received data with the expected data.*/
            if((RedStr[0] != ii)||
              (RedStr[1] != 0x00)||
              (RedStr[2] != 0x00)||
              (RedStr[3] != 0x00))
                  {
                  /*Display error data.*/
                  printf("Error in Channel %d Self-Test Data.\n"
                        "Expected Data = %2X 00 00 00\n"
                        "Received Data = %2X %2X %2X %2X\n",
                        CurChan,ii
                        RedStr[0],RedStr[1],RedStr[2],RedStr[3]);
                  }
            }

      /*Read and compare ARINC words from the Receiver.*/
      for(ii=1; ii <= 0x80; ii<<1)
            {
            /*Read 1 word from the Receiver*/
            RedRX(RedStr,4);

            /*Compare the received data with the expected data.*/
            if((RedStr[0] != 0x00)||
              (RedStr[1] != ii)||
              (RedStr[2] != 0x00)||
              (RedStr[3] != 0x00))
                  {
```

```
            /*Display error data.*/
            printf("Error in Channel %d Self-Test Data.\n"
                    "Expected Data = 00 %2X 00 00\n"
                    "Received Data = %2X %2X %2X %2X\n",
                    CurChan,ii
                    RedStr[0],RedStr[1],RedStr[2],RedStr[3]);
            }
        }

    /*Read and compare ARINC words from the Receiver.*/
    for(ii=1; ii <= 0x80; ii<<1)
        {
        /*Read 1 word from the Receiver*/
        RedRX(RedStr,4);

        /*Compare the received data with the expected data.*/
        if((RedStr[0] != 0x00)||
          (RedStr[1] != 0x00)||
          (RedStr[2] != ii)||
          (RedStr[3] != 0x00))
            {
            /*Display error data.*/
            printf("Error in Channel %d Self-Test Data.\n"
                    "Expected Data = 00 00 %2X 00\n"
                    "Received Data = %2X %2X %2X %2X\n",
                    CurChan,ii
                    RedStr[0],RedStr[1],RedStr[2],RedStr[3]);
            }
        }

    /*Read and compare ARINC words from the Receiver.*/
    for(ii=1; ii <= 0x40; ii<<1)
        {
        /*Read 1 word from the Receiver*/
        RedRX(RedStr,4);

        /*Compare the received data with the expected data.*/
        if((RedStr[0] != 0x00)||
          (RedStr[1] != 0x00)||
          (RedStr[2] != 0x00)||
          (RedStr[3] != ii))
            {
            /*Display error data.*/
            printf("Error in Channel %d Self-Test Data.\n"
                    "Expected Data = 00 00 00 %2X\n"
                    "Received Data = %2X %2X %2X %2X\n",
                    CurChan,ii
                    RedStr[0],RedStr[1],RedStr[2],RedStr[3]);
            }
```

```
            }
        }

    /*End of the example program 4 in C.*/
    }
```

Appendix A
VXIbus Operation

CAUTION

If the user's mainframe has other manufacturer's computer boards operating in the role of VXIbus foreign devices, the assertion of BERR (as defined by the VXIbus Specification) may cause operating problems on these boards.*

The VX4428 Module is a C size single slot VXIbus Message-Based Word Serial instrument. It uses the A16, D16 VME interface available on the backplane P1 connector and does not require any A24 or A32 address space. The module is a D16 interrupter.

The VX4428 Module is neither a VXIbus commander or VMEbus master, and therefore it does not have a VXIbus Signal register. The VX4428 is a VXIbus message based servant.

The module supports the Normal Transfer Mode of the VXIbus, using the Write Ready, Read Ready, Data In Ready (DIR), and Data Out Ready (DOR) bits of the module's Response register.

A Normal Transfer Mode read of the VX4428 Module proceeds as follows:

1. The commander reads the VX4428's Response register and checks if the Write Ready bit is true. If it is, the commander proceeds to the next step. If not, the commander continues to poll this bit until it becomes true.

2. The commander writes the Byte Request command (0DEFFh) to the VX4428's Data Low register.

3. The commander reads the VX4428's Response register and checks if the Read Ready and DOR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll these bits until they become true.

4. The commander reads the VX4428's Data Low register.

A Normal Transfer Mode Write to the VX4428 Module proceeds as follows:

1. The commander reads the VX4428's Response register and checks if the Write Ready and DIR bits are true. If they are, the commander proceeds to the next step. If not, the commander continues to poll the Write Ready and DIR bits until they are true.

2. The commander writes the Byte Available command which contains the data (0BCXX or 0BDXX, depending on the End bit) to the VX4428's Data Low register.

The VX4428 Module has no registers beyond those defined for VXIbus message based devices. All communications with the module are through the Data Low register, the Response register or the VXIbus interrupt cycle. Any attempt by another module to read or write to any undefined location of the VX4428's address space may cause incorrect operation of the module.

As with all VXIbus devices, the VX4428 Module has registers located within a 64 byte block in the A16 address space.

The base address of the VX4428 device's registers is determined by the device's unique logical address and can be calculated as follows:

Base Address = V * 40H + C000H

where V is the device's logical address as set by the Logical Address switches.

VX4428 Configuration Registers

Below is a list of the VX4428 Configuration registers with a complete description of each. In this list, RO = Read Only, WO = Write Only, R = Read, and W = Write. The offset is relative to the module's base address:

REGISTER DEFINITIONS

Register	Address	Type	Value (Bits 15-0)
ID	0000H	RO	1011 1111 1111 1100 (BFFCh)
Logical Address	0000H	WO	See Logical Address definition below
Device Type	0002H	RO	See Device Type definition below
Status	0004H	RO	See Status definition below
Control	0004H	WO	See Control definition below
Offset	0006H	RO	1111 1111 1111 1111 (FFFFh)
Protocol	0008H	RO	1111 0111 1111 1111 (F7FFh)
Response	000AH	RO	Defined by state of the interface
Data High	000CH		Not used
Data Low	000EH	W	See Data Low definition below

REGISTER BIT DEFINITIONS

ID: BFFCh

Device: F7FFh

Protocol: E7FFh

Word Serial Commands

A write to the Data Low register causes this module to execute some action based on the data written. This section describes the device-specific Word Serial commands this module responds to and the results of these commands.

Read Protocol command response: FE6Bh

Appendix B
Input/Output Connections

Signal	Description	VX4428 Signal Pin No.
ARINC I/O Connector:		SI Connector
TX Chan 1 Line A	Trans. Chan. 1 ARINC 429 Line A	12
TX Chan 1 Line B	Trans. Chan. 1 ARINC 429 Line B	13
TX Chan 2 Line A	Trans. Chan. 2 ARINC 429 Line A	9
TX Chan 2 Line B	Trans. Chan. 2 ARINC 429 Line B	10
TX Chan 3 Line A	Trans. Chan. 3 ARINC 429 Line A	6
TX Chan 3 Line B	Trans. Chan. 3 ARINC 429 Line B	7
TX Chan 4 Line A	Trans. Chan. 4 ARINC 429 Line A	3
TX Chan 4 Line B	Trans. Chan. 4 ARINC 429 Line B	4
RX Chan 1 Line A	Receive. Chan. 1 ARINC 429 Line A	24
RX Chan 1 Line B	Receive. Chan. 1 ARINC 429 Line B	23
RX Chan 2 Line A	Receive. Chan. 2 ARINC 429 Line A	21
RX Chan 2 Line B	Receive. Chan. 2 ARINC 429 Line B	20
RX Chan 3 Line A	Receive. Chan. 3 ARINC 429 Line A	18
RX Chan 3 Line B	Receive. Chan. 3 ARINC 429 Line B	17
RX Chan 4 Line A	Receive. Chan. 4 ARINC 429 Line A	14
RX Chan 4 Line B	Receive. Chan. 4 ARINC 429 Line B	15
GND	GROUND	1
GND	GROUND	2
GND	GROUND	5
GND	GROUND	8
GND	GROUND	11
GND	GROUND	16
GND	GROUND	19
GND	GROUND	22
GND	GROUND	25

Signal	Description	VX4428 Signal Pin No.
Trigger I/O Connector:		S2 Connector
TX Trig0Out*	Transmit. Trigger Line 0 Out, Active Low	10
TX Trig1Out*	Transmit. Trigger Line 1 Out, Active Low	9
TX Trig2Out*	Transmit. Trigger Line 2 Out, Active Low	1
TX Trig3Out*	Transmit. Trigger Line 3 Out, Active Low	2
TX Trig0In*	Transmit. Trigger Line 0 In, Active Low	6
TX Trig1In*	Transmit. Trigger Line 1 In, Active Low	5
TX Trig2In*	Transmit. Trigger Line 2 In, Active Low	3
TX Trig3In*	Transmit. Trigger Line 3 In, Active Low	4
RX Trig0Out*	Receiver Trigger Line 0 Out, Active Low	7
RX Trig1Out*	Receiver Trigger Line 1 Out, Active Low	14
RX Trig2Out*	Receiver Trigger Line 2 Out, Active Low	8
RX Trig3Out*	Receiver Trigger Line 3 Out, Active Low	15
GND	GROUND	11
GND	GROUND	12
GND	GROUND	13
Auxiliary Transmitter TTL Output Connector:		S3 Connector
Clk 1 Out	Channel 1 Bit Rate Clock Out	B
Sync 1	Channel 1 Sync Out	C
NRZ 1	Channel 1 NRZ Data Out	D
Data Clk 1	Channel 1 Data Clock Out	E
Clk 2 Out	Channel 2 Bit Rate Clock Out	H
Sync 2	Channel 2 Sync Out	J
NRZ 2	Channel 2 NRZ Data Out	K
Data Clk 2	Channel 2 Data Clock Out	L

Appendix C
VXI Glossary

The terms in this glossary are defined as used in the VXIbus System. Although some of these terms may have different meanings in other systems, it is important to use these definitions in VXIbus applications. Terms which apply only to a particular instrument module are noted. Not all terms appear in every manual.

Term	Definition
Accessed Indicator	An amber LED indicator that lights when the module identity is selected by the Resource Manager module, and flashes during any I/O operation for the module.
ACFAIL*	A VMEbus backplane line that is asserted under these conditions: 1) by the mainframe Power Supply when a power failure has occurred (either ac line source or power supply malfunction), or 2) by the front panel ON/STANDBY switch when switched to STANDBY.
A-Size Card	A VXIbus instrument module that is 100.0 by 160 mm by 20.32 mm (3.9 by 6.3 in by 0.8 in), the same size as a VMEbus single-height short module.
Asynchronous Communication	Communications that occur outside the normal "command-response" cycle. Such communications have higher priority than synchronous communication.
Backplane	The printed circuit board that is mounted in a VXIbus mainframe to provide the interface between VXIbus modules and between those modules and the external system.
B-Size Card	A VXIbus instrument module that is 233.4 by 160 mm by 20.32 mm (9.2 by 6.3 in by 0.8 in), the same size as a VMEbus double-height short module.
Bus Arbitration	In the VMEbus interface, a system for resolving contention for service among VMEbus Master devices on the VMEbus.
Bus Timer	A functional module that measures the duration of each data transfer on the Data Transfer Bus (DTB) and terminates the DTB cycle if the duration is excessive. Without the termination capability of this module, a Bus Master attempt to transfer data to or from a non-existent Slave location could result in an infinitely long wait for the Slave response.

Client — In shared memory protocol (SMP), that half of an SMP channel that does not control the shared memory buffers.

CLK10 — A 10-MHz, ± 100 ppm, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1-12 on P2. It is distributed to each module slot as a single source, single destination signal with a matched delay of under 8 ns.

CLK100 — A 100-MHz, ± 100 ppm, individually buffered (to each module slot), differential ECL system clock that is sourced from Slot 0 and distributed to Slots 1-12 on P3. It is distributed to each module slot in synchronous with CLK10 as a single source, single destination signal with a maximum system timing skew of 2 ns, and a maximum total delay of 8 ns.

Commander — In the VXIbus interface, a device that controls another device (a servant). A commander may be a servant of another commander.

Command — A directive to a device. There are three types of commands:

In Word Serial Protocol, a 16-bit imperative to a servant from its commander.

In Shared Memory Protocol, a 16-bit imperative from a client to a server, or vice versa.

In a Message, an ASCII-coded, multi-byte directive to any receiving device.

Communication Registers — In word serial protocol, a set of device registers that are accessible to the commander of the device. Such registers are used for inter-device communications, and are required on all VXIbus message-based devices.

Configuration Registers — A set of registers that allow the system to identify a (module) device type, model, manufacturer, address space, and memory requirements. In order to support automatic system and memory configuration, the VXIbus standard specifies that all VXIbus devices have a set of such registers, all accessible from P1 on the VMEbus.

C-Size Card — A VXIbus instrument module that is 340.0 by 233.4 mm by 30.48 mm (13.4 by 9.2 in by 1.2 in).

Custom Device — A special-purpose VXIbus device that has configuration registers so as to be identified by the system and to allow for definition of future device types to support further levels of compatibility.

Data Transfer Bus — One of four buses on the VMEbus backplane. The Data Transfer Bus allows Bus Masters to direct the transfer of binary data between Masters and Slaves.

DC SUPPLIES Indicator — A red LED indicator that illuminates when a DC power fault is detected on the backplane.

Device Specific Protocol — A protocol for communication with a device that is not defined in the VXIbus specification.

D-Size Card — A VXIbus instrument module that is 340.0 by 366.7 mm by 30.48 mm (13.4 x 14.4 in x 1.2 in).

DTB — See Data Transfer Bus.

DTB Arbiter — A functional module that accepts bus requests from Requester modules and grants control of the DTB to one Requester at a time.

DUT — Device Under Test.

ECLTRG — Six single-ended ECL trigger lines (two on P2 and four on P3) that function as inter-module timing resources, and that are bussed across the VXIbus subsystem backplane. Any module, including the Slot 0 module, may drive and receive information from these lines. These lines have an impedance of 50 ohms; the asserted state is logical High.

Embedded Address — An address in a communications protocol in which the destination of the message is included in the message.

ESTST — Extended STart/STop protocol; used to synchronize VXIbus modules.

Extended Self Test — Any self test or diagnostic power-up routine that executes after the initial kernel self test program.

External System Controller — The host computer or other external controller that exerts overall control over VXIbus operations.

FAILED Indicator — A red LED indicator that lights when a device on the VXIbus has detected an internal fault. This might result in the assertion of the SYSFAIL* line.

IACK Daisy Chain Driver — The circuit that drives the VMEbus Interrupt Acknowledge daisy chain line that runs continuously through all installed modules or through jumpers across the backplane.

ID-ROM — An NVRAM storage area that provides for non-volatile storage of diagnostic data.

Instrument Module — A plug-in printed circuit board, with associated components and shields, that may be installed in a VXIbus mainframe. An instrument module may contain more than one device. Also, one device may require more than one instrument module.

Interface Device — A VXIbus device that provides one or more interfaces to external equipment.

Interrupt Handler — A functional module that detects interrupt requests generated by Interrupters and responds to those requests by requesting status and identity information.

Interrupter — A device capable of asserting VMEbus interrupts and performing the interrupt acknowledge sequence.

IRQ — The Interrupt ReQuest signal, which is the VMEbus interrupt line that is asserted by an Interrupter to signify to the controller that a device on the bus requires service by the controller.

Local Bus — A daisy-chained bus that connects adjacent VXIbus slots.

Local Controller — The instrument module that performs system control and external interface functions for the instrument modules in a VXIbus mainframe or several mainframes. See Resource Manager.

Local Processor — The processor on an instrument module.

Logical Address — The smallest functional unit recognized by a VXIbus system. It is often used to identify a particular module.

Mainframe — **Card Cage** For example, the Tektronix VX1400A Mainframe, an operable housing that includes 13 C-size VXIbus instrument module slots.

Memory Device — A storage element (such as bubble memory, RAM, and ROM) that has configuration registers and memory attributes (such as type and access time).

Message — A series of data bytes that are treated as a single communication, with a well defined terminator and message body.

Message Based Device — A VXIbus device that supports VXI configuration and communication registers. Such devices support the word serial protocol, and possibly other message-based protocols.

MODID Lines — Module/system identity lines.

Physical Address	The address assigned to a backplane slot during an access.
Power Monitor	A device that monitors backplane power and reports fault conditions.
P1	The top-most backplane connector for a given module slot in a vertical mainframe such as the Tektronix VX1400. The left-most backplane connector for a given slot in a horizontal mainframe.
P2	The bottom backplane connector for a given module slot in a vertical C-size mainframe such as the VX1400; or the middle backplane connector for a given module slot in a vertical D-size mainframe such as the VX1500.
P3	The bottom backplane connector for a given module slot in a vertical D-size mainframe such as the Tektronix VX1500.
Query	A form of command that allows for inquiry to obtain status or data.
READY Indicator	A green LED indicator that lights when the power-up diagnostic routines have been completed successfully. An internal failure or failure of +5-volt power will extinguish this indicator.
Register Based Device	A VXIbus device that supports VXI register maps, but not high level VXIbus communication protocols; includes devices that are register-based servant elements.
Requester	A functional module that resides on the same module as a Master or Interrupt Handler and requests use of the DTB whenever its Master or Interrupt Handler requires it.
Resource Manager	A VXIbus device that provides configuration management services such as address map configuration, determining system hierarchy, allocating shared system resources, performing system self test diagnostics, and initializing system commanders.
Self Calibration	A routine that verifies the basic calibration of the instrument module circuits, and adjusts this calibration to compensate for short- and long-term variables.
Self Test	A set of routines that determine if the instrument module circuits will perform according to a given set of standards. A self test routine is performed upon power-up.
Servant	A VXIbus message-based device that is controlled by a commander.
Server	A shared memory device that controls the shared memory buffers used in a given Shared Memory Protocol channel.

Shared Memory Protocol — A communications protocol that uses a block of memory that is accessible to both client and server. The memory block operates as a message buffer for communications.

Slot 0 Controller — See Slot 0 Module. Also see Resource Manager.

Slot 0 Module — A VXIbus device that provides the minimum VXIbus slot 0 services to slots 1 through 12 (CLK10 and the module identity lines), but that may provide other services such as CLK100, SYNC100, STARBUS, and trigger control.

SMP — See Shared Memory Protocol.

STARX — Two (2) bi-directional, 50 ohm, differential ECL lines that provide for inter-module asynchronous communication. These pairs of timed and matched delay lines connect slot 0 and each of slots 1 through 12 in a mainframe. The delay between slots is less than 5 nanoseconds, and the lines are well matched for timing skew.

STARY — Two (2) bi-directional, 50 ohm, differential ECL lines that provide for inter-module asynchronous communication. These pairs of timed and matched delay lines connect slot 0 and each of slots 1 through 12 in a mainframe. The delay between slots is less than 5 nanoseconds, and the lines are well matched for timing skew.

STST — STart/STop protocol; used to synchronize modules.

SYNC100 — A Slot 0 signal that is used to synchronize multiple devices with respect to a given rising edge of CLK100. These signals are individually buffered and matched to less than 2ns of skew.

Synchronous Communications — A communications system that follows the "command-response" cycle model. In this model, a device issues a command to another device; the second device executes the command; then returns a response. Synchronous commands are executed in the order received.

SYSFAIL* — A signal line on the VMEbus that is used to indicate a failure by a device. The device that fails asserts this line.

System Clock Driver — A functional module that provides a 16-MHz timing signal on the Utility Bus.

System Hierarchy — The tree structure of the commander/servant relationships of all devices in the system at a given time. In the VXIbus structure, each servant has a commander. A commander may also have a commander.

Test Monitor An executive routine that is responsible for executing the self tests, storing any errors in the ID-ROM, and reporting such errors to the Resource Manager.

Test Program A program, executed on the system controller, that controls the execution of tests within the test system.

Test System A collection of hardware and software modules that operate in concert to test a target DUT.

TTLTRG Open collector TTL lines used for inter-module timing and communication.

VXIbus Subsystem One mainframe with modules installed. The installed modules include one module that performs slot 0 functions and a given complement of instrument modules. The subsystem may also include a Resource Manager.

Word Serial Protocol A VXIbus word oriented, bi-directional, serial protocol for communications between message-based devices (that is, devices that include communication registers in addition to configuration registers).

Word Serial Communications Inter-device communications using the Word Serial Protocol.

WSP See Word Serial Protocol.

10-MHz Clock A 10 MHz, ±100 ppm timing reference. Also see CLK10.

100-MHz Clock A 100 MHz, ±100 ppm clock synchronized with CLK10. Also see CLK100.

488-To-VXIbus Interface A message based device that provides for communication between the IEEE-488 bus and VXIbus instrument modules.

Appendix D
User Service

This appendix contains service-related information that covers the following topics:

- Preventive maintenance
- User-replaceable Parts

Preventive Maintenance

You should perform inspection and cleaning as preventive maintenance. Preventive maintenance, when done regularly, may prevent malfunction and enhance reliability. inspect and clean the module as often as conditions require by following these steps:

1. Turn off power and remove the module from the VXIbus mainframe.
2. Remove loose dust on the outside of the instrument with a lint-free cloth.
3. Remove any remaining dirt with lint-free cloth dampened in a general purpose detergent-and-water solution. Do not use abrasive cleaners.

User-Replaceable Parts

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable.

User-Replaceable Parts

Part Description	Part Number
User Manual	070-9145-XX
Label, Tek CDS	950-0926-00
Label, VXI	950-1016-00
Fuse, Micro 4 Amp 125 V Fast	159-0374-00
Fuse, Micro 1 Amp 125 V Fast	159-01164-00
Collar Screw, Metric 2.5 × 11 Slotted	950-0952-00
Shield, Front	950-1324-00
Screw, Phillips Metric 2.5 × 4 FLHD SS	211-0867-00

Appendix E
Option 10

Option 10 to the VX4428 adds the capability to start the time-stamp clock based upon an external trigger input to any or all of the four receiver channels.

The following changes take effect when Option 10 is installed in the VX4428.

Specifications

Front Panel
Trigger Inputs:

Type: TTL, Active Low.
Load: 0.17 milliamps maximum.
Pulse width: 250 nanoseconds minimum.

NOTE: The front panel trigger inputs have a 10,000 ohm pullup resistor installed on each input.

Power-up:

The VX4428 Option 10 receiver defaults to the following states on power-up:

No trigger input selected.

Time-stamp clocks in continuous run mode.

Operation

During normal operation, the VX4428 time-stamp clock starts counting upon execution of the Receiver Enable (RE) command. Option 10 allows holding off the time-stamp clock start until either an external trigger input is received or the user issues a command enabling the clock. The time-stamp value for all data received prior to the reception of the external trigger will be at time zero (0).

Option 10 can be used to synchronize all four channels' time-stamp clocks or to indicate when a particular event has occurred by the time-stamp value incrementing.

Once a channel time-stamp clock has been enabled by reception of an external trigger, the time-stamp clock will be in continuous run mode until disabled by the ET command.

The front-panel trigger inputs added for Option 10 use the front-panel trigger output lines with the addition of 10K ohm pull-up resistors. These resistors eliminate the need to add external resistors for the front-panel trigger outputs.

Module Commands

A summary of the VX4428 Option 10 additional or modified receiver commands is listed below. This is followed by detailed descriptions of each of the commands.

Command	Action
ET	Enable Time-stamp clock - Switches control of the time-stamp clock between the external trigger input and the continuous time-stamp clock.
ID	Return ID - Returns a string containing the module identification and software version to the system controller on its next request for input from the card.
TI	Trigger Input Select - Selects the input trigger line to be used to start the selected channel(s) respective time-stamp clock.

Command Order

The order in which commands are programmed for the VX4428 Option 10 is significant. All receiver channel setup information must be programmed prior to enabling the receivers. This means that the ET and TI commands must be executed prior to sending the RE (Receiver Enable) command to any channel which will be using the triggered time-stamp mode.

Command Descriptions

A detailed description of each command, in alphabetical order, is given on the following pages.

Command: ET (Enable Time-stamp clock)

Syntax: [chan][ena]ET

Purpose: The ET command switches control of the time-stamp clock between the external trigger input and the continuous time-stamp clock.

Description: [chan] is a 1-digit decimal integer that specifies the channels affected by the TI command as follows:

[chan]	Channel(s) Affected
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

[ena] is a 1-digit decimal integer that specifies the current state of the time-stamp clock for the channels specified by [chan].

[ena]	Action
0	The time-stamp clock runs continuously.
1	The time-stamp clock is controlled by the external trigger input specified by the TI command.

The time-stamp clocks are in continuous run mode after power-up or the RS command.

Examples:

1. The command 0ET sets all of the channel time-stamp clocks to continuous run.

2. The command 11ET sets the channel 1 time-stamp clock to halt until the trigger input specified by the TI command is received or until a ET command is received switching the time-stamp clock to continuous mode (such as 11ET).

3. The ET command can also be used to start or stop the time-stamp clock without receiving an external trigger.

   Assume that all of the channel time-stamp clocks were disabled by issuing the 1ET command. Further assume that all of the receivers were enabled using the RE command. By issuing a 0ET command at time X after the receivers were enabled, all of the channel time-stamp clocks would start counting at time X. This allows the user to synchronize the time-stamp clocks of all four channels within 1 clock cycle for the time-stamp resolution selected. (See the TR command in the Operating Manual.)

The time-stamp clocks can also be stopped at time Y after being started. This would allow the data of interest to be the only data with differing time-stamps.

The time-stamp can be started any number of times while the channels are enabled.

NOTE: The preceding example assumes that either the trigger input selection was disconnected or no trigger input was received on the defined trigger line.

Errors: A Syntax error will result if an out-of-range value is specified for [ena].

If a Syntax error is generated when the command is received, the command will be ignored.

Command: ID (Return ID)

Syntax: ID

Purpose: The ID (Return ID) command will cause the VX4428 receiver to return a string containing the module identification and software version to the system controller on its next request for input from the card.

Description: The string returned by this command is:

CDS VX4428 RECEIVER VX.X OPTION 10<CR><LF>

where X.X represents the version of the software.

The ID command will be stopped by receiving an M command or the VXIbus word serial Clear command.

NOTE: Issuing the CD, DS, MM, SC, or SD command before receiving the <CR><LF> will cause the VX4428 receiver to stop the ID command and return to the previously selected data return mode for the active channel.

Errors: A Syntax error will result if a parameter value precedes the command.

If a Syntax error is generated when the command is received, the command will be ignored.

Command: TI (Trigger Input Select)

Syntax: [chan][trgln]TI

Purpose: The TI command selects the input trigger line to be used to start the selected channel(s) respective time-stamp clock.

Description: [chan] is a 1-digit decimal integer that specifies the channels affected by the TI command as follows:

[chan]	Channel(s) Affected
no parameter	1-4
0	1-4
1	1
2	2
3	3
4	4

[trgln] is a 2-digit decimal integer that specifies the front-panel or VXIbus TTL trigger line to be used as the external trigger for the channel(s) defined by [chan]:

[trgln]	Trigger line Selected
00	VXIbus TTL Trigger 0
01	VXIbus TTL Trigger 1
02	VXIbus TTL Trigger 2
03	VXIbus TTL Trigger 3
04	VXIbus TTL Trigger 4
05	VXIbus TTL Trigger 5
06	VXIbus TTL Trigger 6
07	VXIbus TTL Trigger 7
08	Front-panel Trigger 0
09	Front-panel Trigger 1
10	Front-panel Trigger 2
11	Front-panel Trigger 3

If any values other than those listed above are used for the [trgln] parameter, the front-panel and VXIbus TTL trigger lines will be disconnected from the channel(s) defined by [chan]. Once a channel is disconnected from the front panel or VXI TTL trigger lines, the time-stamp clock for that channel may only be enabled with the ET command.

On power-up or after an RS (Reset) command, all trigger input lines are de-selected (disabled).

Examples:

1. The command sequence 101TI selects the VXIbus trigger line 1 as the external trigger input for channel 1.

2. The command sequence 011TI (or 11TI) selects the front-panel trigger line 3 as the external trigger input for all channels.

Errors: A syntax error will result if an out-of-range value is specified for [chan] or if the number of characters for both the [chan] and [trgln] parameters is more than 3 characters.

If a syntax error is generated when the command is received, the command will be ignored.

Appendix F: Binary Transfer

If you are using a National Instruments GPIB-VXI/C Slot 0 module and are planning on using the binary transfer capabilities of the modules above, you will need to load a CI (Code Instrument) into the GPIB-VXI/C Slot 0.

***NOTE**. The GPIB-VXI/C Slot 0 has an internal buffer that holds the data to be read out. The buffer will automatically take a reading from the module upon a GPIB read. The buffer will read the module until it receives an END BIT (bit 8 set in the response to a byte request command). The Tektronix products above do not set bit 8 on readback, thus the GPIB-VXI/C Slot 0 will fill its buffer with data (approximately 450 Kbytes). If you only request 1 Kbytes of data over GPIB there still will be 449 Kbytes of data in the buffer. This data will remain in the buffer until read out. If you should request data from another module the data that you will receive back will be from the data that is left over in the buffer (449 Kbytes).*

National Instruments has developed a code instrument that will read the exact number of bytes that was requested over the GPIB bus from the module. The code instrument will not read more data then requested and will have no leftover data in the buffer. Refer to the National Instruments GPIB-VXI/C manual for information on code instruments.

If you need any assistance call 1-800-TEK-WIDE or contact your local Tektronix representative.

Appendix G: Performance Verification Procedure

This procedure verifies the performance of the 73A-425 (ARINC 429 Quad Transmitter), 73A-426 (ARINC 429 Quad Receiver), and VX4428 (ARINC 429 Quad Transmitter/Receiver) module. You may perform the verification in your current VXIbus system if it meets the minimum requirements specified in paragraph labeled Required Equipment. It is not necessary to complete the entire procedure if you are only interested in a specific performance area. However, the verification of some parameters rely on the correct operation of previously validated functions so follow the order presented.

Conventions Used In This Procedure

Please familiarize yourself with the following conventions which apply throughout this procedure:

- Each of the voltage and bit tests are accompanied with an example to help you visualize what the signal must look like. Whenever the signal has changed you will be given a new example of a valid signal.
- Programming of the module assumes no particular interface. The manual lists the ASCII commands that need to be sent to the module and it is up to you to form the commands properly of the interface that you use.
- The procedure will check one of the four channels of the 73A-425 and 73A-426 first, then instruct you to repeat the procedure for the other channels. If you are using the 73A-426 module then you will need a 73A-425 module to check the receiver.
- In this manual you will see reference to hexadecimal words (0XFF). When ever this is encountered the meaning is to send out a 8-bit byte with the hex value shown:

    - Example 1, BASIC program:
      wrt$ = “1L”+CHR$(255)+CHR$(255)+CHR$(255)+CHR$(127)

    - Example 2, “C” program:
      sprintf(wrt,”1L%c%c%c%c”,0XFF,0XFF,0XFF,0X7F);

Prerequisites

The verification sequences in this procedure are valid when the following requirements are met:

- The 73A-425/73A-426/VX4428 has passed its power-on self test.
- All covers are in place and the module is installed in an approved VXIbus mainframe according to the instructions in the INSTALLATION section of the Operating Manual.
- The 73A-425/73A-426/VX4428 has been operating for a warm-up period of at least ten minutes and is operating in an ambient environment as specified in the *SPECIFICATIONS* section of the Operating Manual.

Equipment Required

Table 1–1 lists the equipment required for the performance and verification procedure.

Table 1–1: Equipment Required

Required tools and equipment	Part number
VXI Mainframe (such as the Tektronix VX1410)	n/a
VXI Slot 0 with resource Manager (Tektronix VX4521) and appropriate cables and interface cards.	n/a
Digitizing Oscilloscope with at least a 500 MHz bandwidth and a sample frequency of 1 GHz with a minimum of 2-channels.	n/a
25-pin male DB connector (used to connect transmitter to receiver)	n/a
15 pin male DB connector for S2	n/a
A cable to connect 73A-425 Channel 1 Transmitter to all four 73A-426 Receiver channels.	
Talker/Listener (Send/Read) program with the capability to send and read binary data, and send word serial commands.	n/a
A cable to connect the channel 1 transmitter to all four receiver channels S1 pin-12 to S1 pins-24, 21, 18, 14. S1 pin-13 to S1 pins-23, 20, 17, 15. Temporarily jumper S2 Pin-10 to Pin-5, Pin-9 to Pin-3, Pin-1 to Pin-4, and Pin-2 to Pin-6. This will supply a 5 V pull up voltage for the trig out pins from the trig in pins and will allow checking triggers. [1]	n/a
A cable to connect the four 73A-425 Transmitter channels to the four 73A-426 Receiver channels. This cable will need to have TNC Triax connector on each end. Be sure and make a place to connect an Oscilloscope probe to Line A and Line B. Mark which connection is for Line A or Line B. The center connector is line A, the outer connector is line B, the shell is ground. Temporarily jumper S7 Pin-2 to Pin-1, Pin-5 to Pin-8, Pin-7 to Pin-6, and Pin-9 to Pin-4. This will supply a 5 V pull-up voltage for the trig out pins from the trig in pins and will allow checking triggers.[2]	n/a
Talker/Listener (send/read) program with the capabilities to send out binary values in the range of 0x00 to 0xFF, along with ASCII data. This program will also need to be able to send/read word serial commands to/from the instrument.	

[1] **Required for VX4428 check out only**

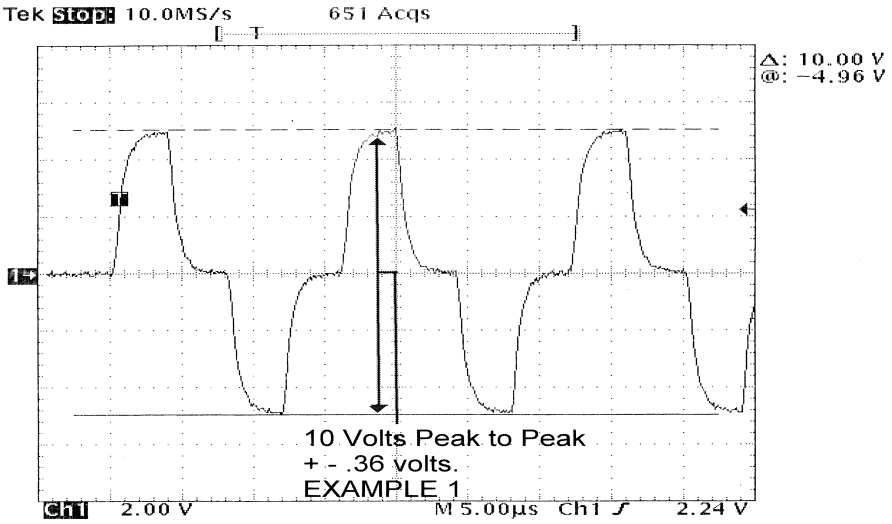
[2] **Required for 73A-426 check out only**

Transmitter Test

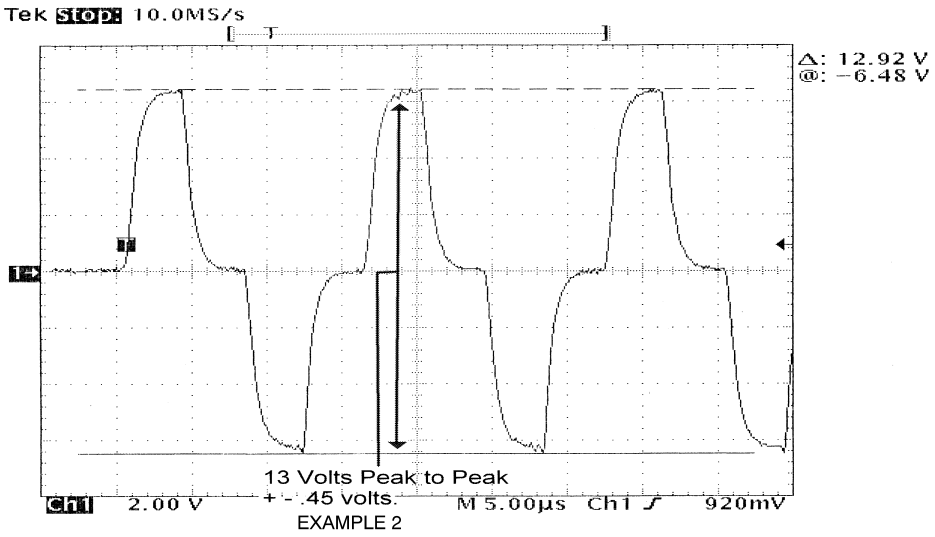
1. Send the following commands to the 73A-425 or Transmitter side of the VX4428.
   Note that <cr/lf> means carriage return and line feed characters.
   - **a.** K<cr/lf>
   - **b.** T
   - **c.** Wait approximately 28 seconds.
   - **d.** E
2. Read back the error code from the 73A-425 or Transmitter side of the VX4428. The error code will be “99”. A return of “NO ERRORS” or any other response is a failure.

Voltage Amplitude Test

1. Connect Oscilloscope channel 1 to pin-12 of S1 on the VX4428 or to LINE A channel 1 on the cable for the 73A-425. Set the time base switch to 5.00 Microseconds and the vertical switch to 2.00 V.
2. Send the following commands to the 73A-425 or Transmitter side of the VX4428.
   - **a.** 1S<cr/lf>
   - **b.** 0A<cr/lf>
   - **c.** 40R<cr/lf>
   - **d.** 3L+0x80+0x00+0x00+0x80+0x55+0x55+0x55+0x55+0x00+0x00+0x40+0x80<cr/lf>
   - **e.** 0V<cr/lf>
   - **f.** 1D<cr/lf>
   - **g.** 1B<cr/lf>
3. Measure the peak-to-peak value of the signal on Channel 1. It must be 10.00 V ± 0.36 V, and have the same waveform as shown in Example 1.

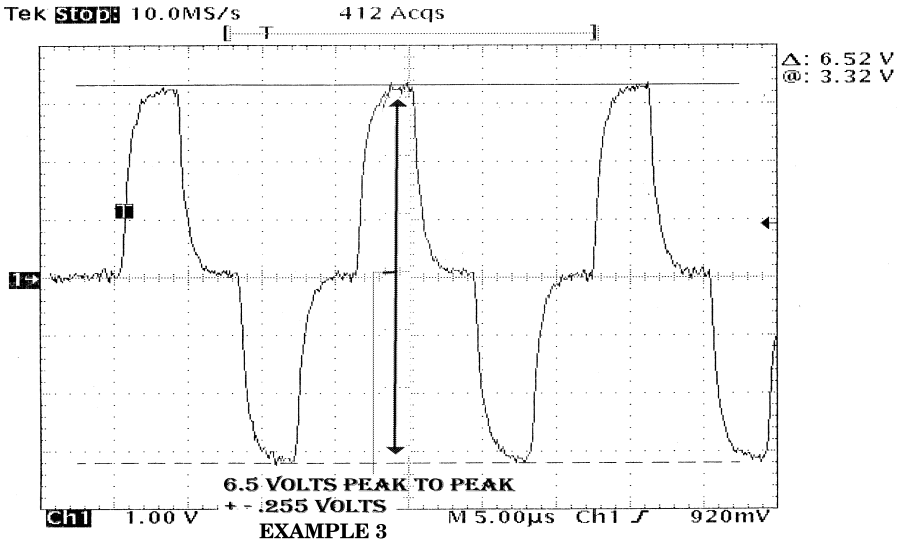


4. Connect Oscilloscope channel 1 to pin-13 of S1 on the VX4428 or to LINE B on the cable for the 73A-425.
5. Measure the peak-to-peak value of the signal on Channel 1. It must be 10.00 V ± 0.36 V. See Example 1.
6. Send the following commands to the 73A-425 or Transmitter side of the VX4428.
   a. 1Q<cr/lf>
   b. 0A<cr/lf>
   c. 1V<cr/lf>
   d. 1B<cr/lf>
7. Connect Oscilloscope channel 1 to pin-12 of S1 on the VX4428 or to LINE A channel 1 on the cable for the 73A-425.
8. Measure the peak-to-peak value of the signal on Channel 1. It must be 13.00 V ± 0.45 V. See Example 2.



EXAMPLE 2

9. Connect Oscilloscope channel 1 to pin-13 of S1 on the VX4428 or to LINE B channel 1 on the cable for the 73A-425.
10. Measure the peak-to-peak value of the signal on Channel 1. It must be 13.00 V ± 0.45 V. See Example 2.
11. Send the following commands to the 73A-425 or Transmitter side of the VX4428.
   a. 1Q<cr/lf>
   b. 0A<cr/lf>
   c. 2V<cr/lf>
   d. 1B<cr/lf>
12. Connect Oscilloscope channel 1 to pin-12 of S1 on the VX4428 or to LINE A channel 1 on the cable for the 73A-425.
13. Measure the peak-to-peak value of the signal on Channel 1. It must be 6.50 V ± 0.255 V. See Example 3.



14. Connect Osc. channel 1 to pin 13 of S1 on the VX4428 or to LINE B channel 1 on the cable for the 73A–425.

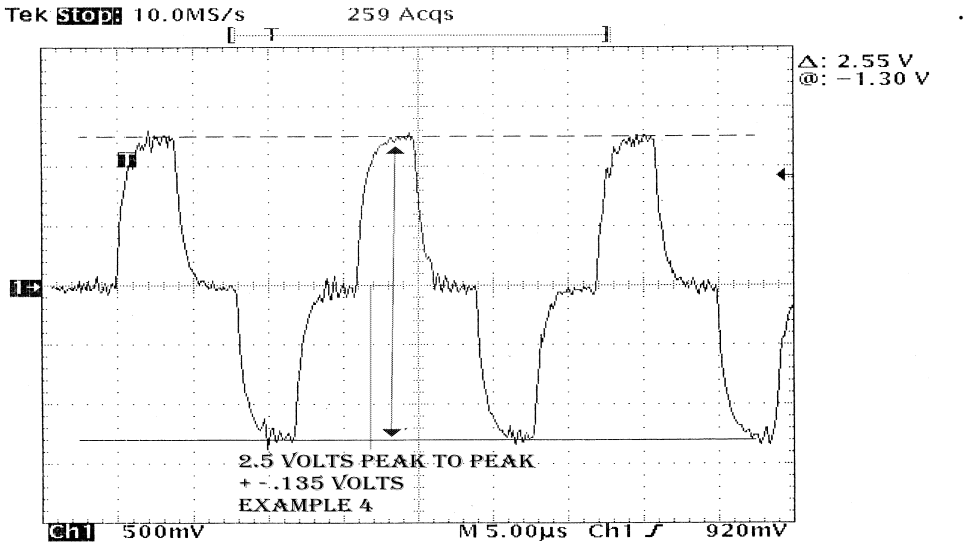
15. Measure the peak-to-peak value of the signal on Channel 1. It should be 6.50 volts ±.255 Volts. See Example 3.

16. Send the following commands to the 73A–425 or Transmitter side of the VX4428.

- **a.** 1Q<cr/lf>
- **b.** 0A<cr/lf>
- **c.** 3V<cr/lf>
- **d.** 1B<cr/lf>

17. Connect Osc. channel 1 to pin 12 of S1 on the VX4428 or to LINE A channel 1 on the cable for the 73A–425.

18. Measure the peak-to-peak value of the signal on Channel 1. It should be 2.50 volts ±0.135 Volts. See Example 4.



19. Connect Osc. channel 1 to pin 13 of S1 on the VX4428 or to LINE B channel 1 on the cable for the 73A–425.

20. Measure the peak-to-peak value of the signal on Channel 1. It should be 2.50 volts ± 0.135 Volts. See Example 4.

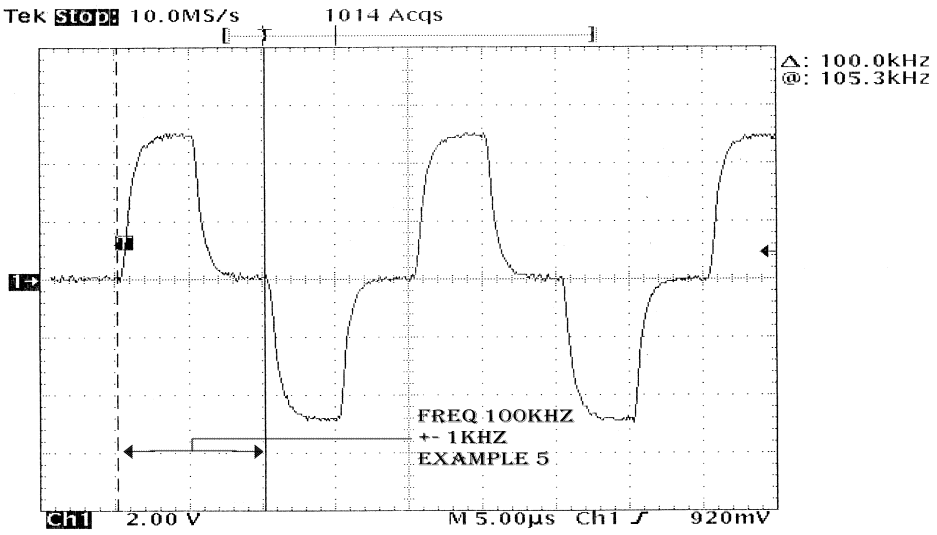
TRANSMITTER FREQUENCY TEST CHANNEL 1

1. Send the following commands to the 73A–425 or Transmitter side of the VX4428.

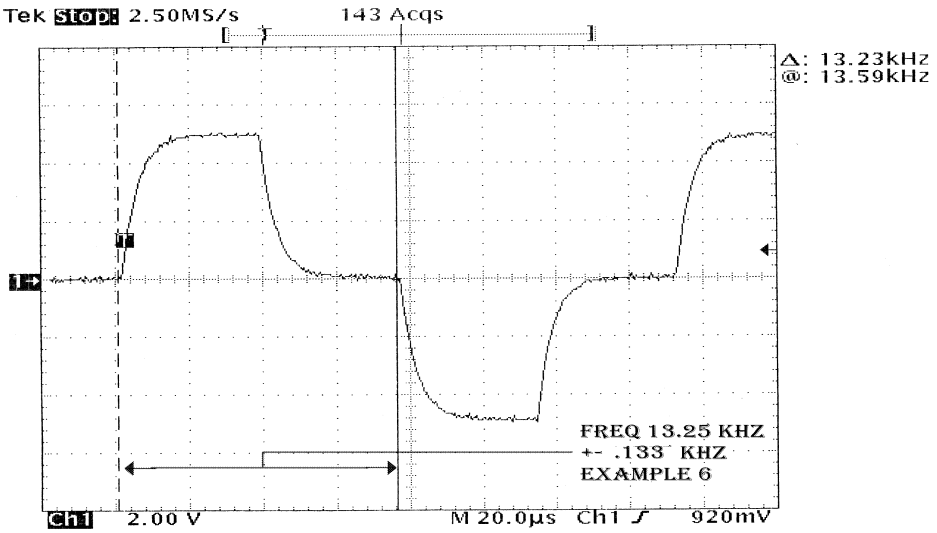
- **a.** 1Q<cr/lf>
- **b.** 0A<cr/lf>
- **c.** 40R<cr/lf>
- **d.** 0V<cr/lf>
- **e.** 1B<cr/lf>

2. Connect Osc. channel 1 to pin 12 of S1 on the VX4428 or to LINE A channel 1 on the cable for the 73A–425.

3. Measure the frequency of the peak-to-peak signal on Channel 1. It should be 100 kHz ±1 kHz. See Example 5.

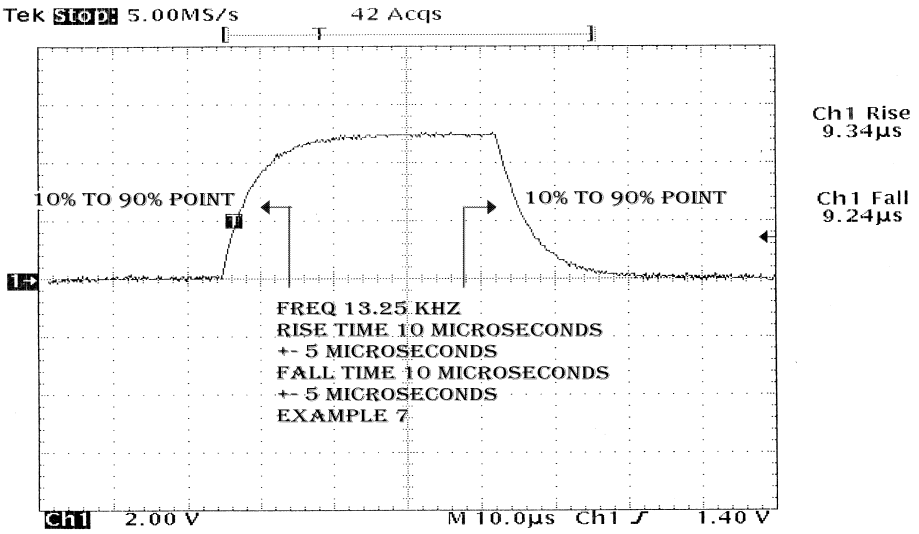


4. Send the following commands to the 73A–425 or Transmitter side of the VX4428.
   - **a.** 1Q<cr/lf>
   - **b.** 0A<cr/lf>
   - **c.** 302R<cr/lf>
   - **d.** 0V<cr/lf>
   - **e.** 1B<cr/lf
5. Connect Osc. channel 1 to pin 12 of S1 on the VX4428 or to LINE A channel 1 on the cable for the 73A–425.
6. Measure the frequency of the peak-to-peak signal on Channel 1. It should be 13.25 Khz ±133 hz. See Example 6.

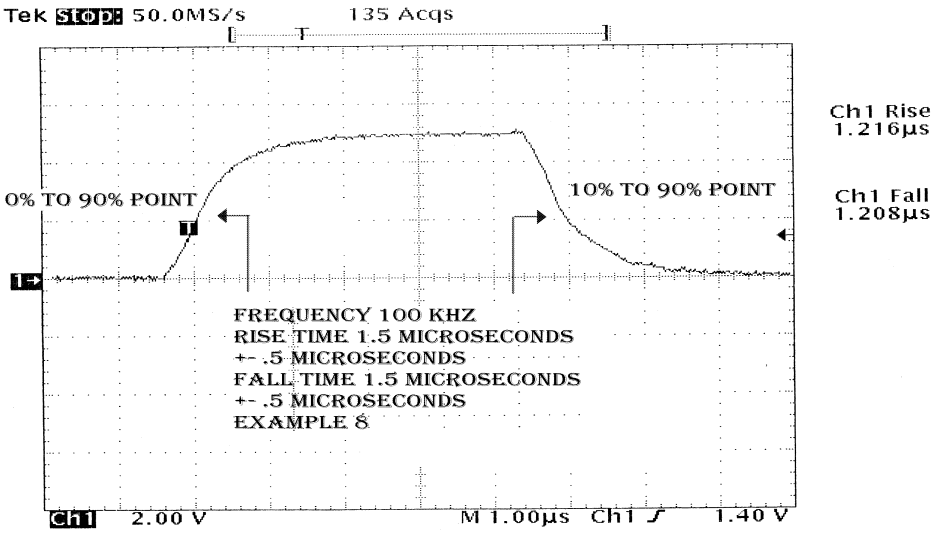


RISE/FALL TIME TEST CHANNEL 1

1. Send the following commands to the 73A–425 or Transmitter side of the VX4428.
   - **a.** 1Q<cr/lf>
   - **b.** 0A<cr/lf>
   - **c.** 0V<cr/lf>
   - **d.** 1B<cr/lf>
2. Connect Osc. channel 1 to pin 12 of S1 on the VX4428 or to LINE A channel 1 on the cable for the 73A–425.
3. Measure the rise and fall time of the peak-to-peak signal on Channel 1. The rise/fall time should be 10 Microseconds + – 5 Microseconds. See Example 7.

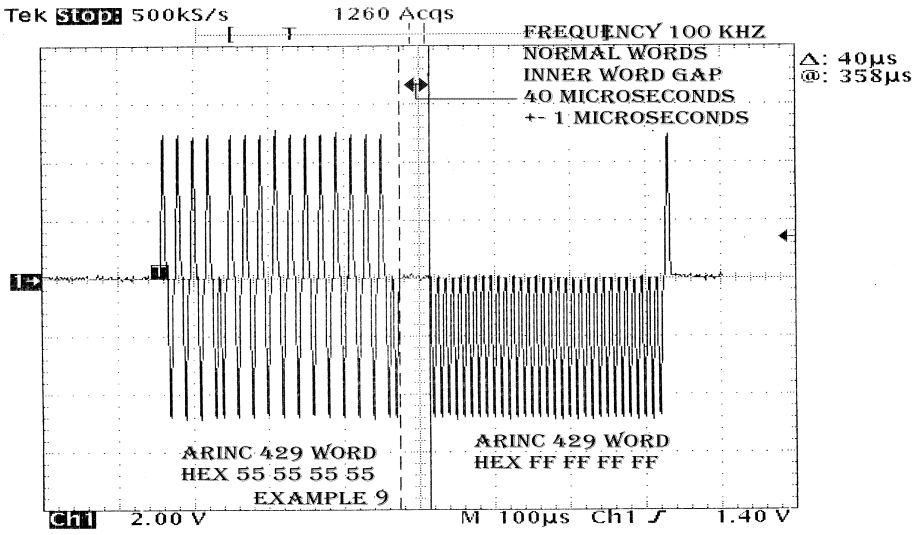


4. Send the following commands to the 73A–425 or Transmitter side of the VX4428.
   - **a.** 1Q<cr/lf>
   - **b.** 0A<cr/lf>
   - **c.** 40R<cr/lf>
   - **d.** 1B<cr/lf>
5. Connect Osc. channel 1 to pin 12 of S1 on the VX4428 or to LINE A channel 1 on the cable for the 73A–425.
6. Measure the rise and fall time of the peak-to-peak signal on Channel 1. The rise/fall time should be 1.5 Microseconds ±0 .5 Microseconds. See Example 8.


Tek Stop: 50.0MS/s
135 Acqs
Ch1 Rise
1.216µs
0% TO 90% POINT
10% TO 90% POINT
Ch1 Fall
1.208µs
FREQUENCY 100 KHZ
RISE TIME 1.5 MICROSECONDS
+- .5 MICROSECONDS
FALL TIME 1.5 MICROSECONDS
+- .5 MICROSECONDS
EXAMPLE 8
Ch1 2.00 V
M 1.00µs Ch1 ƒ 1.40 V

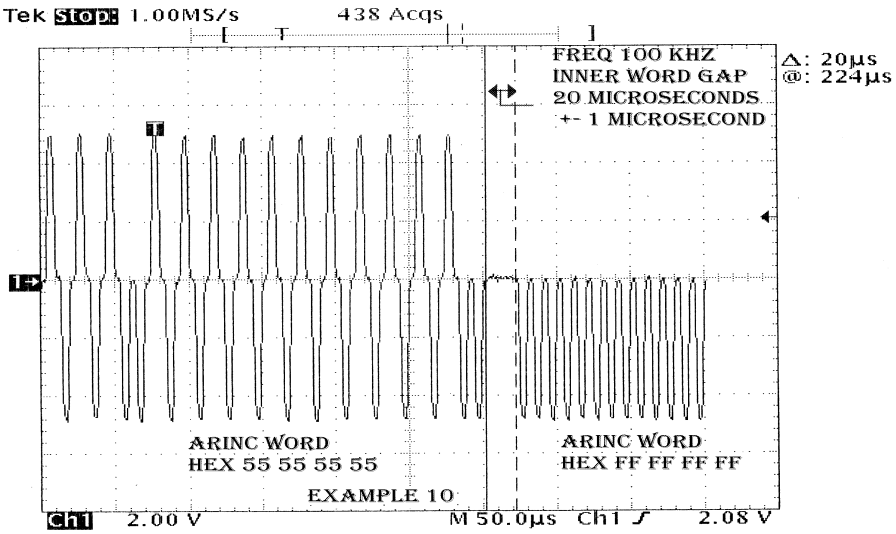
Interword Gap Test

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428.
   - **a.** K<cr/lf>
   - **b.** 1S<cr/lf>
   - **c.** 0A<cr/lf>
   - **d.** 40R<cr/lf>
   - **e.** 4L+0x80+0x00+0x00+0x80+0x55+0x55+0x55+0x55+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   - **f.** 0V<cr/lf>
   - **g.** 1D<cr/lf>
   - **h.** 1B<cr/lf>
2. Connect Oscilloscope channel 1 to pin-12 of S1 on the VX4428 or to LINE A channel 1 on the cable for the 73A-425.
3. Measure the interword gap time of the signal on Channel 1.
   The gap time is 40 Microseconds ± 1 Microsecond. See Example 9.



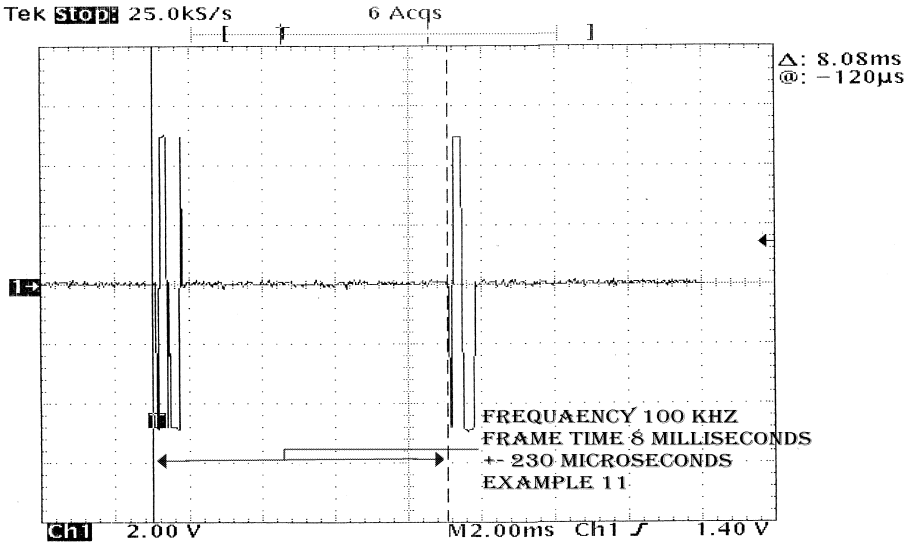
4. Send the following commands to the 73A-425 or Transmitter side of the VX4428.
   - **a.** K<cr/lf>
   - **b.** 1S<cr/lf>
   - **c.** 0A<cr/lf>
   - **d.** 40R<cr/lf>
   - **e.** 4L+0x80+0x00+0x08+0x80+0x55+0x55+0x55+0x55+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   - **f.** 0V<cr/lf>
   - **g.** 1D<cr/lf>
   - **h.** 1B<cr/lf>

5. Connect Oscilloscope channel 1 to pin-12 of S1 on the VX4428 or to LINE A channel 1 on the cable for the 73A-425.
6. Measure the interword gap time of the signal on Channel 1.
   The gap-time is 20 Microseconds ± 1 Microsecond. See Example 10.



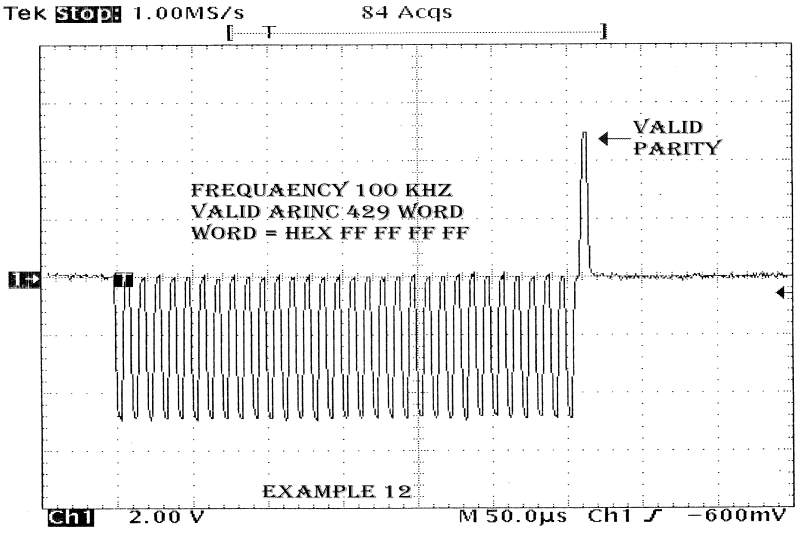
Frame Time Test

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428.
   - **a.** K<cr/lf>
   - **b.** 1S<cr/lf>
   - **c.** 0A<cr/lf>
   - **d.** 40R<cr/lf>
   - **e.** 4L+0x80+0x00+0x00+0x80+0x55+0x55+0x55+0x55+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   - **f.** 0V<cr/lf>
   - **g.** 1D<cr/lf>
   - **h.** 1B<cr/lf>
2. Connect Oscilloscope channel 1 to pin-12 of S1 on the VX4428 or to LINE A channel 1 on the cable for the 73A-425.
3. Measure the frame time of the signal on Channel 1.
   The frame time is 8 Milliseconds ± 230 Microsecond. See Example 11.



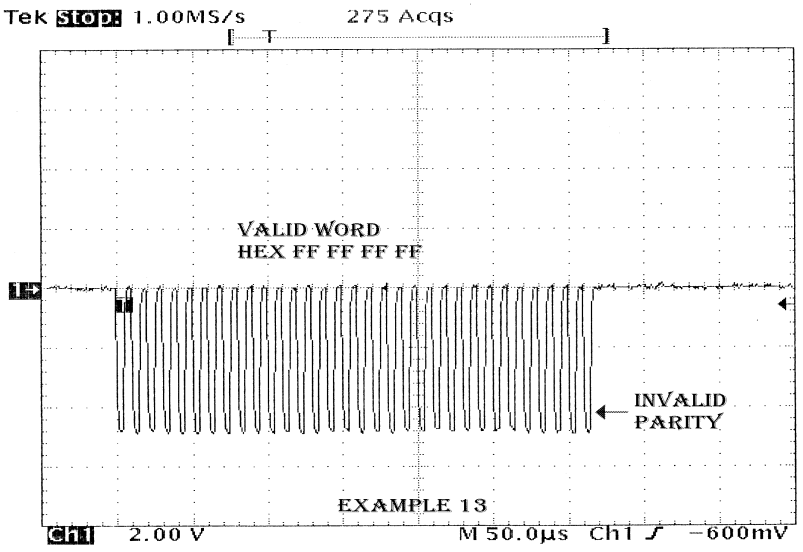
Valid ARINC Word Test

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428.
   a. K<cr/lf>
   b. 1S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x00+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 1D<cr/lf>
   h. 1B<cr/lf>
2. Connect Oscilloscope channel 1 to pin-12 of S1 on the VX4428 or to LINE A channel 1 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for valid Parity (odd parity is valid). See Example 12.



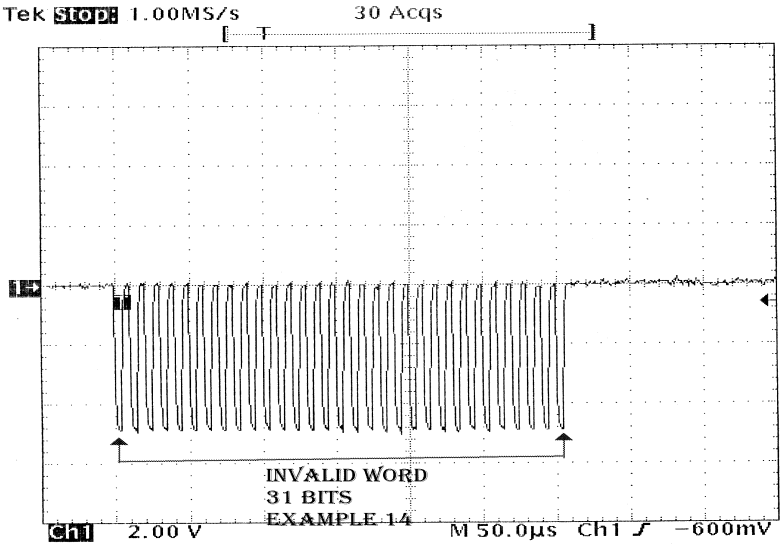
Incorrect Parity Test

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428.
   - **a.** K<cr/lf>
   - **b.** 1S<cr/lf>
   - **c.** 0A<cr/lf>
   - **d.** 40R<cr/lf>
   - **e.** 3L+0x80+0x00+0x01+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   - **f.** 0V<cr/lf>
   - **g.** 1D<cr/lf>
   - **h.** 1B<cr/lf>
2. Connect Oscilloscope channel 1 to pin-12 of S1 on the VX4428 or to LINE A channel 1 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for invalid Parity (odd parity is valid). See Example 13.



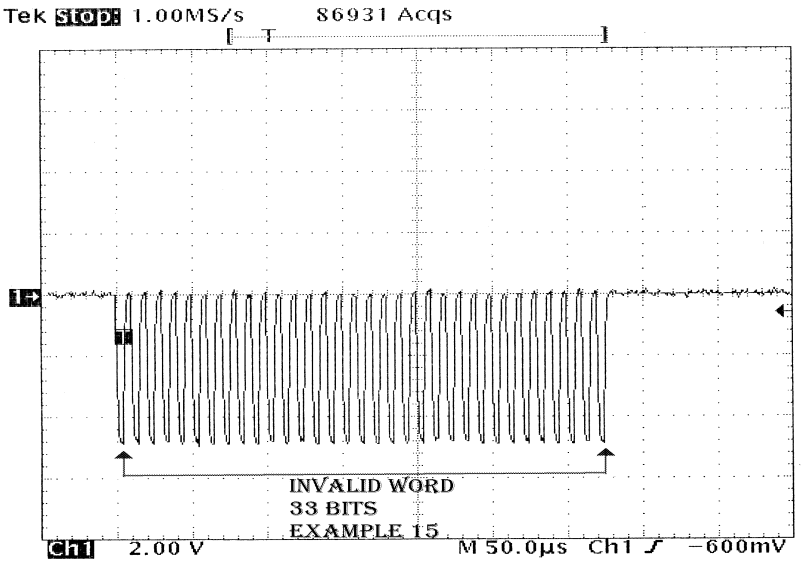
31-Bit ARINC Word Test

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428.
   - **a.** K<cr/lf>
   - **b.** 1S<cr/lf>
   - **c.** 0A<cr/lf>
   - **d.** 40R<cr/lf>
   - **e.** 3L+0x80+0x00+0x02+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   - **f.** 0V<cr/lf>
   - **g.** 1D<cr/lf>
   - **h.** 1B<cr/lf>
2. Connect Oscilloscope channel 1 to pin-12 of S1 on the VX4428 or to LINE A channel 1 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for a word with 31-bits. See Example 14.



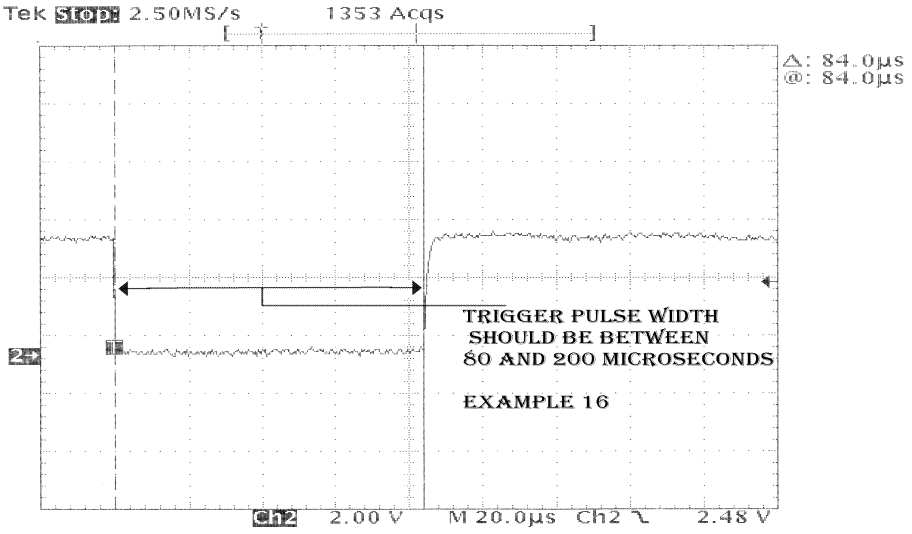
33-Bit ARINC Word Test

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428.
   - **a.** K<cr/lf>
   - **b.** 1S<cr/lf>
   - **c.** 0A<cr/lf>
   - **d.** 40R<cr/lf>
   - **e.** 3L+0x80+0x00+0x04+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   - **f.** 0V<cr/lf>
   - **g.** 1D<cr/lf>
   - **h.** 1B<cr/lf>
2. Connect Oscilloscope channel 1 to pin-12 of S1 on the VX4428 or to LINE A channel 1 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for a word with 33-bits. See Example 15.



Trigger Output Pulse Width Test

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428.
   - **a.** K<cr/lf>
   - **b.** 1S<cr/lf>
   - **c.** 0A<cr/lf>
   - **d.** 40R<cr/lf>
   - **e.** 3L+0x80+0x00+0x10+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   - **f.** 0V<cr/lf>
   - **g.** 118F<cr/lf>
   - **h.** 1D<cr/lf>
   - **i.** 1B<cr/lf>
2. Connect Oscilloscope channel 1 to pin-10 of S2 on the VX4428 or to S7 Pin 2 on the 73A-425.
3. Check the waveform on Channel 1 for a negative going pulse that is between 80 Microseconds and 200 Microseconds wide. See Example 16.



TTL Trigger Test

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 2S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x00+0x80+0xAA+0x55+0x55+0x55+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 200X<cr/lf>
   h. 2D<cr/lf>
   i. 2P<cr/lf>
   j. Connect oscilloscope channel 1 to pin 12 of S1 on the VX4428 or to LINE A Channel 1 of 73A-425.
   k. Connect oscilloscope channel 2 to pin 9 of S1 on the VX4428 or to LINE A Channel 2 of 73A-425.
   l. Check and make sure that their is no ARINC word being transmitted on Channel 2.
2. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 1S<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 3L+0x80+0x00+0x10+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   e. 0V<cr/lf>
   f. 110F<cr/lf>
   g. 1D<cr/lf>
   h. 1B<cr/lf>
3. Check and make sure that their are ARINC words being transmitted on Channel 1 and Channel 2.

Front Panel Trigger Test

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 2S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x00+0x80+0xAA+0x55+0x55+0x55+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 209X<cr/lf>
   h. 2D<cr/lf>
   i. 2P<cr/lf>
2. Connect oscilloscope channel 1 to pin 12 of S1 on the VX4428 or to LINE A Channel 1 of 73A-425.

3. Connect oscilloscope channel 2 to pin 9 of S1 on the VX4428 or to LINE A Channel 2 of 73A-425.
4. Check and make sure that their is no ARINC word being transmitted on Channel 2.
5. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 1S<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 3L+0x80+0x00+0x10+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   e. 0V<cr/lf>
   f. 118F<cr/lf>
   g. 1D<cr/lf>
   h. 1B<cr/lf>
6. Check and make sure that their is ARINC words being transmitted on Channel 1 and Channel 2.
7. Send the following command to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>

Voltage Amplitude Test Channel 2

1. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A channel 2 on the cable for the 73A-425. Set the time base switch to 5.00 Microseconds and the vertical switch to 2.00 V.
2. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 2S<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 3L+0x80+0x00+0x00+0x80+0x55+0x55+0x55+0x55+0x00+0x00+0x40+0x80<cr/lf>
   e. 0V<cr/lf>
   f. 2D<cr/lf>
   g. 2B<cr/lf>
3. Measure the peak-to-peak value of the signal on Channel 1. It will be 10.00 V ± 0.36 V. See Example 1.
4. Connect oscilloscope channel 1 to pin 10 of S1 on the VX4428 or to LINE B Channel 2 on the cable for the 73A-425.
5. Measure the peak-to-peak value of the signal on Channel 1. It will be 10.00 V ± 0.36 V. See Example 1.
6. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 2Q<cr/lf>
   b. 0A<cr/lf>
   c. 1V<cr/lf>
   d. 2B<cr/lf>
7. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A channel 2 on the cable for the 73A-425.

8. Measure the peak-to-peak value of the signal on Channel 1. It will be 13.00 V ± 0.45 V. See Example 2.
9. Connect oscilloscope channel 1 to pin 10 of S1 on the VX4428 or to LINE B channel 2 on the cable for the 73A-425.
10. Measure the peak-to-peak value of the signal on Channel 1. It will be 13.00 V ± 0.45 V. See Example 2.
11. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
    a. 2Q<cr/lf>
    b. 0A<cr/lf>
    c. 2V<cr/lf>
    d. 2B<cr/lf>
12. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A channel 2 on the cable for the 73A-425.
13. Measure the peak-to-peak value of the signal on Channel 1. It will be 6.50 V ± 0.255 V. See Example 3.
14. Connect oscilloscope channel 1 to pin 10 of S1 on the VX4428 or to LINE B channel 2 on the cable for the 73A-425.
15. Measure the peak-to-peak value of the signal on Channel 1. It will be 6.50 V ± 0.255 V. See Example 3.
16. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
    a. 2Q<cr/lf>
    b. 0A<cr/lf>
    c. 3V<cr/lf>
    d. 2B<cr/lf>
17. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A channel 2 on the cable for the 73A-425.
18. Measure the peak-to-peak value of the signal on Channel 1. It will be 2.50 V ± 0.135 V. See Example 4.
19. Connect oscilloscope channel 1 to pin 10 of S1 on the VX4428 or to LINE B channel 2 on the cable for the 73A-425.
20. Measure the peak-to-peak value of the signal on Channel 1. It will be 2.50 V ± 0.135 V. See Example 4.

Transmitter Frequency Test Channel 2

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 2Q<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 0V<cr/lf>
   e. 2B<cr/lf>
2. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A channel 2 on the cable for the 73A-425.
3. Measure the frequency of the peak-to-peak signal on Channel 1. It will be 100 Khz ± 1 Khz. See Example 5.
4. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 2Q<cr/lf>
   b. 0A<cr/lf>
   c. 302R<cr/lf>
   d. 0V<cr/lf>
   e. 2B<cr/lf>
5. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A channel 2 on the cable for the 73A-425.
6. Measure the frequency of the peak-to-peak signal on Channel 1. It will be 13.25 Khz ± 133 Hz. See Example 6.

Rise/Fall Time Test Channel 2

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 2Q<cr/lf>
   b. 0A<cr/lf>
   c. 0V<cr/lf>
   d. 2B<cr/lf>
2. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A channel 2 on the cable for the 73A-425.
3. Measure the rise and fall time of the peak-to-peak signal on Channel 1. The rise/fall time will be 10 Microseconds ± 5 Microseconds. See Example 7.
4. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 2Q<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 2B<cr/lf>
5. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A channel 2 on the cable for the 73A-425.
6. Measure the rise and fall time of the peak-to-peak signal on Channel 1. The rise/fall time will be 1.5 Microseconds ± 0.5 Microseconds. See Example 8.

Interword Gap Test Channel 2

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 2S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 4L+0x80+0x00+0x00+0x80+0x55+0x55+0x55+0x55+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 2D<cr/lf>
   h. 2B<cr/lf>
2. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A channel 2 on the cable for the 73A-425.
3. Measure the interword gap time of the signal on Channel 1. The gap time is 40 Microseconds ± 1 Microsecond. See Example 9.
4. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 2S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 4L+0x80+0x00+0x08+0x80+0x55+0x55+0x55+0x55+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 2D<cr/lf>
   h. 2B<cr/lf>
5. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A channel 2 on the cable for the 73A-425.
6. Measure the interword gap time of the signal on Channel 1. The gap time is 20 Microseconds ± 1 Microsecond. See Example 10.

Frame Time Test Channel 2

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 2S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 4L+0x80+0x00+0x00+0x80+0x55+0x55+0x55+0x55+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 2D<cr/lf>
   h. 2B<cr/lf>

2. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A CHANNEL 2 on the cable for the 73A-425.
3. Measure the frame time of the signal on Channel 1. The frame time is 8 Milliseconds ± 230 Microseconds. See Example 11.

Valid ARINC Word Test Channel 2

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 2S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x00+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 2D<cr/lf>
   h. 2B<cr/lf>
2. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A channel 2 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for valid Parity (ODD PARITY IS VALID). See Example 12.

Incorrect Parity Test Channel 2

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 2S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x01+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 2D<cr/lf>
   h. 2B<cr/lf>
2. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A channel 2 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for invalid Parity(ODD PARITY IS VALID). See Example 13.

31-Bit ARINC Word Test Channel 2

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   - **a.** K<cr/lf>
   - **b.** 2S<cr/lf>
   - **c.** 0A<cr/lf>
   - **d.** 40R<cr/lf>
   - **e.** 3L+0x80+0x00+0x02+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   - **f.** 0V<cr/lf>
   - **g.** 2D<cr/lf>
   - **h.** 2B<cr/lf>
2. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A channel 2 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for a word with 31 bits. See Example 14.

33-Bit ARINC Word Test Channel 2

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   - **a.** K<cr/lf>
   - **b.** 2S<cr/lf>
   - **c.** 0A<cr/lf>
   - **d.** 40R<cr/lf>
   - **e.** 3L+0x80+0x00+0x04+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   - **f.** 0V<cr/lf>
   - **g.** 2D<cr/lf>
   - **h.** 2B<cr/lf>
2. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A channel 2 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for a word with 33 bits. See Example 15.

Trigger Output Pulse Width Test Channel 2

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   - **a.** K<cr/lf>
   - **b.** 2S<cr/lf>
   - **c.** 0A<cr/lf>
   - **d.** 40R<cr/lf>
   - **e.** 3L+0x80+0x00+0x10+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   - **f.** 0V<cr/lf>
   - **g.** 228F<cr/lf>
   - **h.** 2D<cr/lf>
   - **i.** 2B<cr/lf>

2. Connect oscilloscope channel 1 to pin 9 of S2 on the VX4428 or to S7 Pin 5 on the 73A-425.
3. Check the waveform on Channel 1 for a negative going pulse that is between 80 Microseconds and 200 Microseconds wide. See Example 16.

TTL Trigger Test Channel 2

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 3S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x00+0x80+0xAA+0x55+0x55+0x55+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 301X<cr/lf>
   h. 3D<cr/lf>
   i. 3P<cr/lf>
2. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A Channel 2 of 73A-425.
3. Connect oscilloscope channel 2 to pin 6 of S1 on the VX4428 or to LINE A Channel 3 of 73A-425.
4. Check and make sure that their is no ARINC word being transmitted on Channel 3.
5. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 2S<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 3L+0x80+0x00+0x10+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   e. 0V<cr/lf>
   f. 221F<cr/lf>
   g. 2D<cr/lf>
   h. 2B<cr/lf>
6. Check and make sure that their is ARINC words being transmitted on Channel 2 and Channel 3.

Front Panel Trigger Test Channel 2

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 3S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x00+0x80+0xAA+0x55+0x55+0x55+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 310X<cr/lf>
   h. 2D<cr/lf>
   i. 2P<cr/lf>
2. Connect oscilloscope channel 1 to pin 9 of S1 on the VX4428 or to LINE A Channel 2 of 73A-425.
3. Connect oscilloscope channel 2 to pin 6 of S1 on the VX4428 or to LINE A Channel 3 of 73A-425.
4. Check and make sure that their is no ARINC word being transmitted on Channel 3.
5. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 2S<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 3L+0x80+0x00+0x10+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   e. 0V<cr/lf>
   f. 228F<cr/lf>
   g. 2D<cr/lf>
   h. 2B<cr/lf>
6. Check and make sure that their is ARINC words being transmitted on Channel 2 and Channel 3.
7. Send the following command to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>

Voltage Amplitude Test Channel 3

1. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A channel 3 on the cable for the 73A-425. Set the time base switch to 5.00 Microseconds and the vertical switch to 2.00 V.
2. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 3S<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 3L+0x80+0x00+0x00+0x80+0x55+0x55+0x55+0x55+0x00+0x00+0x40+0x80<cr/lf>
   e. 0V<cr/lf>

f. 3D<cr/lf>

g. 3B<cr/lf>

3. Measure the peak-to-peak value of the signal on Channel 1. It will be 10.00 V ± 0.36 V. See Example 1.

4. Connect oscilloscope channel 1 to pin 7 of S1 on the VX4428 or to LINE B Channel 3 on the cable for the 73A-425.

5. Measure the peak-to-peak value of the signal on Channel 1. It will be 10.00 V ± 0.36 V. See Example 1.

6. Send the following commands to the 73A-425 or Transmitter side of the VX4428:

a. 3Q<cr/lf>

b. 0A<cr/lf>

c. 1V<cr/lf>

d. 3B<cr/lf>

7. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A channel 3 on the cable for the 73A-425.

8. Measure the peak-to-peak value of the signal on Channel 1. It will be 13.00 V ± 0.45 V. See Example 2.

9. Connect oscilloscope channel 1 to pin 7 of S1 on the VX4428 or to LINE B channel 3 on the cable for the 73A-425.

10. Measure the peak-to-peak value of the signal on Channel 1. It will be 13.00 V ± 0.45 V. See Example 2.

11. Send the following commands to the 73A-425 or Transmitter side of the VX4428:

a. 3Q<cr/lf>

b. 0A<cr/lf>

c. 2V<cr/lf>

d. 3B<cr/lf>

12. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A channel 3 on the cable for the 73A-425.

13. Measure the peak-to-peak value of the signal on Channel 1. It will be 6.50 V ± 0.255 V. See Example 3.

14. Connect oscilloscope channel 1 to pin 7 of S1 on the VX4428 or to LINE B channel 3 on the cable for the 73A-425.

15. Measure the peak-to-peak value of the signal on Channel 1. It will be 6.50 V ± 0.255 V. See Example 3.

16. Send the following commands to the 73A-425 or Transmitter side of the VX4428:

a. 3Q<cr/lf>

b. 0A<cr/lf>

c. 3V<cr/lf>

d. 3B<cr/lf>

17. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A channel 3 on the cable for the 73A-425.

18. Measure the peak-to-peak value of the signal on Channel 1. It will be 2.50 V ± 0.135 V. See Example 4.

19. Connect oscilloscope channel 1 to pin 7 of S1 on the VX4428 or to LINE B channel 3 on the cable for the 73A-425.
20. Measure the peak-to-peak value of the signal on Channel 1. It will be 2.50 V ± 0.135 V. See Example 4.

Transmitter Frequency Test Channel 3

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 3Q<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 0V<cr/lf>
   e. 3B<cr/lf>
2. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A channel 3 on the cable for the 73A-425.
3. Measure the frequency of the peak-to-peak signal on Channel 1. It will be 100 Khz ± 1 Khz. See Example 5.
4. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 3Q<cr/lf>
   b. 0A<cr/lf>
   c. 302R<cr/lf>
   d. 0V<cr/lf>
   e. 3B<cr/lf>
5. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A channel 3 on the cable for the 73A-425.
6. Measure the frequency of the peak-to-peak signal on Channel 1. It will be 13.25 Khz ± 133 Hz. See Example 6.

Rise/Fall Time Test Channel 3

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 3Q<cr/lf>
   b. 0A<cr/lf>
   c. 0V<cr/lf>
   d. 3B<cr/lf>
2. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A channel 3 on the cable for the 73A-425.
3. Measure the rise and fall time of the peak-to-peak signal on Channel 1. The rise/fall time will be 10 Microseconds ± 5 Microseconds. See Example 7.
4. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 3Q<cr/lf>
   b. 0A<cr/lf>

c. 40R<cr/lf>
d. 3B<cr/lf>

5. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A channel 3 on the cable for the 73A-425.
6. Measure the rise and fall time of the peak-to-peak signal on Channel 1. The rise/fall time will be 1.5 Microseconds ± 0.5 Microseconds. See Example 8.

Interword Gap Test Channel 3

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 3S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 4L+0x80+0x00+0x00+0x80+0x55+0x55+0x55+0x55+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 3D<cr/lf>
   h. 3B<cr/lf>
2. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A channel 3 on the cable for the 73A-425.
3. Measure the interword gap time of the signal on Channel 1. The gap time is 40 Microseconds ± 1 Microsecond. See Example 9.
4. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 3S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 4L+0x80+0x00+0x08+0x80+0x55+0x55+0x55+0x55+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 3D<cr/lf>
   h. 3B<cr/lf>
5. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A channel 3 on the cable for the 73A-425.
6. Measure the interword gap time of the signal on Channel 1. The gap time is 20 Microseconds ± 1 Microsecond. See Example 10.

Frame Time Test Channel 3

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 3S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 4L+0x80+0x00+0x00+0x80+0x55+0x55+0x55+0x55+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 3D<cr/lf>
   h. 3B<cr/lf>
2. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A channel 3 on the cable for the 73A-425.
3. Measure the frame time of the signal on Channel 1. The frame time is 8 Milliseconds ± 230 Microseconds. See Example 11.

Valid ARINC Word Test Channel 3

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 3S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x00+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 3D<cr/lf>
   h. 3B<cr/lf>
2. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A channel 3 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for valid Parity(ODD PARITY IS VALID). See Example 12.

Incorrect Parity Test Channel 3

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 3S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x01+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>

g. 3D<cr/lf>
h. 3B<cr/lf>

2. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A channel 3 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for invalid Parity(ODD PARITY IS VALID). See Example 13.

31-Bit ARINC Word Test Channel 3

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 3S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x02+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 3D<cr/lf>
   h. 3B<cr/lf>
2. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A channel 3 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for a word with 31 bits. See Example 14.

33-Bit ARINC Word Test Channel 3

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 3S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x04+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 3D<cr/lf>
   h. 3B<cr/lf>
2. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A channel 3 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for a word with 33 bits. See Example 15.

Trigger Output Pulse Width Test Channel 3

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 3S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x10+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 338F<cr/lf>
   h. 3D<cr/lf>
   i. 3B<cr/lf>
2. Connect oscilloscope channel 1 to pin 1 of S2 on the VX4428 or to S7 Pin 7 on the 73A-425.
3. Check the waveform on Channel 1 for a negative going pulse that is between 80 Microseconds and 200 Microseconds wide. See Example 16.

TTL Trigger Test Channel 3

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 4S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x00+0x80+0xAA+0x55+0x55+0x55+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 402X<cr/lf>
   h. 4D<cr/lf>
   i. 4P<cr/lf>
2. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A Channel 3 of 73A-425.
3. Connect oscilloscope channel 2 to pin 3 of S1 on the VX4428 or to LINE A Channel 4 of 73A-425.
4. Check and make sure that their is no ARINC word being transmitted on Channel 4.
5. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 3S<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 3L+0x80+0x00+0x10+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   e. 0V<cr/lf>
   f. 332F<cr/lf>
   g. 3D<cr/lf>
   h. 3B<cr/lf>

6. Check and make sure that their is ARINC words being transmitted on Channel 3 and Channel 4.

Front Panel Trigger Test Channel 3

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 4S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x00+0x80+0xAA+0x55+0x55+0x55+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 411X<cr/lf>
   h. 4D<cr/lf>
   i. 4P<cr/lf>
2. Connect oscilloscope channel 1 to pin 6 of S1 on the VX4428 or to LINE A Channel 3 of 73A-425.
3. Connect oscilloscope channel 2 to pin 3 of S1 on the VX4428 or to LINE A Channel 4 of 73A-425.
4. Check and make sure that their is no ARINC word being transmitted on Channel 4.
5. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 3S<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 3L+0x80+0x00+0x10+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   e. 0V<cr/lf>
   f. 338F<cr/lf>
   g. 3D<cr/lf>
   h. 3B<cr/lf>
6. Check and make sure that their is ARINC words being transmitted on Channel 3 and Channel 4.
7. Send the following command to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>

Voltage Amplitude Test Channel 4

1. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A channel 4 on the cable for the 73A-425. Set the time base switch to 5.00 Microseconds and the vertical switch to 2.00 V.
2. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 4S<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>

d. 3L+0x80+0x00+0x00+0x80+0x55+0x55+0x55+0x55+0x00+0x00+0x40+0x80<cr/lf>
e. 0V<cr/lf>
f. 4D<cr/lf>
g. 4B<cr/lf>

3. Measure the peak-to-peak value of the signal on Channel 1. It will be 10.00 V ± 0.36 V. See Example 1.
4. Connect oscilloscope channel 1 to pin 4 of S1 on the VX4428 or to LINE B Channel 4 on the cable for the 73A-425.
5. Measure the peak-to-peak value of the signal on Channel 1. It will be 10.00 V ± 0.36 V. See Example 1.
6. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
a. 4Q<cr/lf>
b. 0A<cr/lf>
c. 1V<cr/lf>
d. 4B<cr/lf>
7. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A channel 4 on the cable for the 73A-425.
8. Measure the peak-to-peak value of the signal on Channel 1. It will be 13.00 V ± 0.45 V. See Example 2.
9. Connect oscilloscope channel 1 to pin 4 of S1 on the VX4428 or to LINE B channel 4 on the cable for the 73A-425.
10. Measure the peak-to-peak value of the signal on Channel 1. It will be 13.00 V ± 0.45 V. See Example 2.
11. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
a. 4Q<cr/lf>
b. 0A<cr/lf>
c. 2V<cr/lf>
d. 4B<cr/lf>
12. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A channel 4 on the cable for the 73A-425.
13. Measure the peak-to-peak value of the signal on Channel 1. It will be 6.50 V ± 0.255 V. See Example 3.
14. Connect oscilloscope channel 1 to pin 4 of S1 on the VX4428 or to LINE B channel 4 on the cable for the 73A-425.
15. Measure the peak-to-peak value of the signal on Channel 1. It will be 6.50 V ± 0.255 V. See Example 3.
16. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
a. 4Q<cr/lf>
b. 0A<cr/lf>
c. 3V<cr/lf>
d. 4B<cr/lf>
17. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A channel 4 on the cable for the 73A-425.

18. Measure the peak-to-peak value of the signal on Channel 1. It will be 2.50 V ± 0.135 V. See Example 4.
19. Connect oscilloscope channel 1 to pin 4 of S1 on the VX4428 or to LINE B channel 4 on the cable for the 73A-425.
20. Measure the peak-to-peak value of the signal on Channel 1. It will be 2.50 V ± 0.135 V. See Example 4.

Transmitter Frequency Test Channel 4

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 4Q<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 0V<cr/lf>
   e. 4B<cr/lf>
2. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A channel 4 on the cable for the 73A-425.
3. Measure the frequency of the peak-to-peak signal on Channel 1. It will be 100 Khz ± 1 Khz. See Example 5.
4. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 4Q<cr/lf>
   b. 0A<cr/lf>
   c. 302R<cr/lf>
   d. 0V<cr/lf>
   e. 4B<cr/lf>
5. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A channel 4 on the cable for the 73A-425.
6. Measure the frequency of the peak-to-peak signal on Channel 1. It will be 13.25 Khz ± 133 Hz. See Example 6.

Rise/Fall Time Test Channel 4

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 4Q<cr/lf>
   b. 0A<cr/lf>
   c. 0V<cr/lf>
   d. 4B<cr/lf>
2. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A channel 4 on the cable for the 73A-425.
3. Measure the rise and fall time of the peak-to-peak signal on Channel 1. The rise/fall time will be 10 Microseconds ± 5 Microseconds. See Example 7.

4. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 4Q<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 4B<cr/lf>
5. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A channel 4 on the cable for the 73A-425.
6. Measure the rise and fall time of the peak-to-peak signal on Channel 1. The rise/fall time will be 1.5 Microseconds ± 0.5 Microseconds. See Example 8.

Interword Gap Test Channel 4

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 4S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 4L+0x80+0x00+0x00+0x80+0x55+0x55+0x55+0x55+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 4D<cr/lf>
   h. 4B<cr/lf>
2. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A channel 4 on the cable for the 73A-425.
3. Measure the interword gap time of the signal on Channel 1. The gap time is 40 Microseconds ± 1 Microsecond. See Example 9.
4. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 4S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 4L+0x80+0x00+0x08+0x80+0x55+0x55+0x55+0x55+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 4D<cr/lf>
   h. 4B<cr/lf>
5. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A channel 4 on the cable for the 73A-425.
6. Measure the interword gap time of the signal on Channel 1. The gap time is 20 Microseconds ± 1 Microsecond. See Example 10.

Frame Time Test Channel 4

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 4S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 4L+0x80+0x00+0x00+0x80+0x55+0x55+0x55+0x55+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 4D<cr/lf>
   h. 4B<cr/lf>
2. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A channel 4 on the cable for the 73A-425.
3. Measure the frame time of the signal on Channel 1. The frame time is 8 Milliseconds ± 230 Microsecond. See Example 11.

Valid ARINC Word Test Channel 4

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 4S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x00+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 4D<cr/lf>
   h. 4B<cr/lf>
2. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A channel 4 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for valid Parity (ODD PARITY IS VALID). See Example 12.

Incorrect Parity test Channel 4

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 4S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x01+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>

g. 4D<cr/lf>
h. 4B<cr/lf>

2. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A channel 4 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for invalid Parity(ODD PARITY IS VALID). See Example 13.

31-Bit ARINC Word Test Channel 4

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 4S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x02+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 4D<cr/lf>
   h. 4B<cr/lf>
2. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A channel 4 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for a word with 31 bits. See Example 14.

22-Bit ARINC Word Test Channel 4

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 4S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x04+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 4D<cr/lf>
   h. 4B<cr/lf>
2. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A channel 4 on the cable for the 73A-425.
3. Check the waveform on Channel 1 for a word with 33 bits. See Example 15.

Trigger Output Pulse Width Test Channel 4

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 4S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x10+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 448F<cr/lf>
   h. 4D<cr/lf>
   i. 4B<cr/lf>
2. Connect oscilloscope channel 1 to pin 2 of S2 on the VX4428 or to S7 Pin 9 on the 73A-425.
3. Check the waveform on Channel 1 for a negative going pulse that is between 80 Microseconds and 200 Microseconds wide. See Example 16.

TTL Trigger Test Channel 4

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 1S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x00+0x80+0xAA+0x55+0x55+0x55+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 103X<cr/lf>
   h. 1D<cr/lf>
   i. 1P<cr/lf>
2. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A Channel 4 of 73A-425.
3. Connect oscilloscope channel 2 to pin 12 of S1 on the VX4428 or to LINE A Channel 1 of 73A-425.
4. Check and make sure that their is no ARINC word being transmitted on Channel 1.
5. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 4S<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 3L+0x80+0x00+0x10+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   e. 0V<cr/lf>
   f. 443F<cr/lf>
   g. 4D<cr/lf>
   h. 4B<cr/lf>

6. Check and make sure that their is ARINC words being transmitted on Channel 4 and Channel 1.

Front Panel Trigger Test Channel 4

1. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>
   b. 1S<cr/lf>
   c. 0A<cr/lf>
   d. 40R<cr/lf>
   e. 3L+0x80+0x00+0x00+0x80+0xAA+0x55+0x55+0x55+0x00+0x00+0x40+0x80<cr/lf>
   f. 0V<cr/lf>
   g. 108X<cr/lf>
   h. 1D<cr/lf>
   i. 1P<cr/lf>
2. Connect oscilloscope channel 1 to pin 3 of S1 on the VX4428 or to LINE A Channel 4 of 73A-425.
3. Connect oscilloscope channel 2 to pin 12 of S1 on the VX4428 or to LINE A Channel 1 of 73A-425.
4. Check and make sure that their is no ARINC word being transmitted on Channel 1.
5. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 4S<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 3L+0x80+0x00+0x10+0x80+0xFF+0xFF+0xFF+0x7F+0x00+0x00+0x40+0x80<cr/lf>
   e. 0V<cr/lf>
   f. 448F<cr/lf>
   g. 4D<cr/lf>
   h. 4B<cr/lf>
6. Check and make sure that their is ARINC words being transmitted on Channel 4 and Channel 1.
7. Send the following command to the 73A-425 or Transmitter side of the VX4428:
   a. K<cr/lf>

Receiver Testing

After completing the Transmitter test, perform the following test to verify the receiver operations:

VX4428 Only. Connect the cable that has transmitter Channel 1 connected to all Receiver channels.

73A-426 Only. Using a 73A-425 Transmitter that has passed the transmitter test, connect the cable that has 73A-425 Transmitter Channel 1 connect to all of the Receiver Channels on the 73A-426.

Receiver Built-In Self Test

1. Send the following commands to the 73A-426 or Receiver side of the VX4428:
   a. RS<cr/lf>
   b. ST
2. Wait approximately 23 seconds, and then send the following command to the 73A-426 or Receiver side of the VX4428:
   a. ER<cr/lf>
3. Read back the error code from the 73A-426 or Receiver side of the VX4428.
4. The error code will be 99 “NO ERRORS”, if error code is not 99 then the unit has failed.

Monitor Mode

1. Send the following commands to the 73A-426 or Receiver side of the VX4428:
   a. RS<cr/lf>
   b. 0TR<cr/lf>
   c. 1SC<cr/lf>
   d. 1BR<cr/lf>
   e. 0MM<cr/lf>
   f. 0DS<cr/lf>
   g. 2SD<cr/lf>
   h. 2SC<cr/lf>
   i. 1BR<cr/lf>
   j. 0MM<cr/lf>
   k. 0DS<cr/lf>
   l. 2SD<cr/lf>
   m. 3SC<cr/lf>
   n. 1BR<cr/lf>
   o. 0MM<cr/lf>
   p. 0DS<cr/lf>
   q. 2SD<cr/lf>
   r. 4SC<cr/lf>
   s. 1BR<cr/lf>
   t. 0MM<cr/lf>
   u. 0DS<cr/lf>
   v. 2SD<cr/lf>
   w. 0RC<cr/lf>
   x. 0RE<cr/lf>
2. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 1S<cr/lf>
   b. 0A<cr/lf>
   c. 40R<cr/lf>
   d. 3L+0x80+0x00+0x00+0x80+0x55+0x55+0x55+0x55+0x00+0x00+0x80+0x80<cr/lf>

e. 0V<cr/lf>
f. 1D<cr/lf>
g. 1B<cr/lf>

3. Wait approximately 1 second then send the following commands to the Receiver:
a. 1SC<cr/lf>
b. 2SD<cr/lf>

4. Read back data from Channel 1 of the Receiver. You will receive back the following six bytes:
Binary hex 01,00,55,55,55,D5

5. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
a. 2SC<cr/lf>
b. 2SD<cr/lf>

6. Read back data from Channel 2 of the Receiver. You will receive back the following six bytes:
Binary hex 01, 00, 55, 55, 55, D5

7. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
a. 3SC<cr/lf>
b. 2SD<cr/lf>

8. Read back data from Channel 3 of the Receiver. You will receive back the following six bytes:
Binary hex 01,00,55,55,55,D5

9. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
a. 4SC<cr/lf>
b. 2SD<cr/lf>

10. Read back data from Channel 4 of the Receiver. You will receive back the following six bytes:
Binary hex 01,00,55,55,55,D5

11. Send the following command to the 73A-425 or Transmitter side of the VX4428:
a. EX<cr/lf>

12. Read back data from the status command to the Receiver. You will receive the following three bytes:
Binary Hex 00,0D,0A

Monitor Mode 31-Bit Error

1. Send the following commands to the 73A-426 or Receiver side of the VX4428:
   - **a.** RS<cr/lf>
   - **b.** 0TR<cr/lf>
   - **c.** 1SC<cr/lf>
   - **d.** 1BR<cr/lf>
   - **e.** 0MM<cr/lf>
   - **f.** 0DS<cr/lf>
   - **g.** 2SD<cr/lf>
   - **h.** 2SC<cr/lf>
   - **i.** 1BR<cr/lf>
   - **j.** 0MM<cr/lf>
   - **k.** 0DS<cr/lf>
   - **l.** 2SD<cr/lf>
   - **m.** 3SC<cr/lf>
   - **n.** 1BR<cr/lf>
   - **o.** 0MM<cr/lf>
   - **p.** 0DS<cr/lf>
   - **q.** 2SD<cr/lf>
   - **r.** 4SC<cr/lf>
   - **s.** 1BR<cr/lf>
   - **t.** 0MM<cr/lf>
   - **u.** 0DS<cr/lf>
   - **v.** 2SD<cr/lf>
   - **w.** 0RC<cr/lf>
   - **x.** 0RE<cr/lf>
2. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   - **a.** 1S<cr/lf>
   - **b.** 0A<cr/lf>
   - **c.** 40R<cr/lf>
   - **d.** 3L+0x80+0x00+0x02+0x80+0x55+0x55+0x55+0x55+0x00+0x00+0x40+0x80<cr/lf>
   - **e.** 0V<cr/lf>
   - **f.** 1D<cr/lf>
   - **g.** 1B<cr/lf>
3. Wait approximately 1 second then send the following commands to the Receiver.
   - **a.** 1SC<cr/lf>
   - **b.** 2SD<cr/lf>
4. Read back data from Channel 1 of the Receiver. You will receive back the following six bytes:

   Binary hex 01,00,55,55,55,00
5. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   - **a.** 2SC<cr/lf>

b. 2SD<cr/lf>

6. Read back data from Channel 2 of the Receiver. You will receive back the following six bytes:

Binary hex 01,00,55,55,55,00

7. Send the following commands to the 73A-425 or Transmitter side of the VX4428:

a. 3SC<cr/lf>

b. 2SD<cr/lf>

8. Read back data from Channel 3 of the Receiver. You will receive back the following six bytes:

Binary hex 01,00,55,55,55,00

9. Send the following commands to the 73A-425 or Transmitter side of the VX4428:

a. 4SC<cr/lf>

b. 2SD<cr/lf>

10. Read back data from Channel 4 of the Receiver. You will receive back the following six bytes:

Binary hex 01,00,55,55,55,00

11. Send the following command to the 73A-425 or Transmitter side of the VX4428:

a. EX<cr/lf>

12. Read back data from the status command to the Receiver. You will receive the following three bytes:

Binary Hex AA,0D,0A

Monitor Mode 33-Bit Error

1. Send the following commands to the 73A-426 or Receiver side of the VX4428:

a. RS<cr/lf>

b. 0TR<cr/lf>

c. 1SC<cr/lf>

d. 1BR<cr/lf>

e. 0MM<cr/lf>

f. 0DS<cr/lf>

g. 2SD<cr/lf>

h. 2SC<cr/lf>

i. 1BR<cr/lf>

j. 0MM<cr/lf>

k. 0DS<cr/lf>

l. 2SD<cr/lf>

m. 3SC<cr/lf>

n. 1BR<cr/lf>

o. 0MM<cr/lf>

p. 0DS<cr/lf>

q. 2SD<cr/lf>

r. 4SC<cr/lf>

s. 1BR<cr/lf>
t. 0MM<cr/lf>
u. 0DS<cr/lf>
v. 2SD<cr/lf>
w. 0RC<cr/lf>
x. 0RE<cr/lf>

2. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
a. 1S<cr/lf>
b. 0A<cr/lf>
c. 40R<cr/lf>
d. 3L+0x80+0x00+0x04+0x80+0x55+0x55+0x55+0x55+0x00+0x00+0x80+0x80<cr/lf>
e. 0V<cr/lf>
f. 1D<cr/lf>
g. 1B<cr/lf>

3. Wait approximately 1 second then send the following commands to the Receiver.
a. 1SC<cr/lf>
b. 2SD<cr/lf>

4. Read back data from Channel 1 of the Receiver.
5. You need to read at least two ARINC words.
6. You will receive back the following 12 bytes:
Binary hex 01,00,55,55,55,00
Binary hex 01,00,00,00,00,00
a. 2SC<cr/lf>
b. 2SD<cr/lf>

7. Read back data from Channel 2 of the Receiver.
8. You need to read at least two ARINC words.
9. You will receive back the following 12 bytes:
Binary hex 01,00,55,55,55,00
Binary hex 01,00,00,00,00,00
a. 3SC<cr/lf>
b. 2SD<cr/lf>

10. Read back data from Channel 3 of the Receiver.
11. You need to read at least two ARINC words.
12. You will receive back the following 12 bytes:
Binary hex 01,00,55,55,55,00
Binary hex 01,00,00,00,00,00
a. 4SC<cr/lf>
b. 2SD<cr/lf>

13. Read back data from Channel 4 of the Receiver.
14. You need to read at least two ARINC words.
15. You will receive back the following 12 bytes:
Binary hex 01,00,55,55,55,00

Binary hex 01,00,00,00,00,00

16. Send the following command to the 73A-426 or Receiver side of the VX4428:
    a. EX<cr/lf>
17. Read back data from the status command to the Receiver.
18. You will receive the following three bytes:
    Binary Hex AA,0D,0A

Monitor Mode Even Parity Error

1. Send the following commands to the 73A-426 or Receiver side of the VX4428:
    a. RS<cr/lf>
    b. 0TR<cr/lf>
    c. 1SC<cr/lf>
    d. 1BR<cr/lf>
    e. 0MM<cr/lf>
    f. 0DS<cr/lf>
    g. 2SD<cr/lf>
    h. 2SC<cr/lf>
    i. 1BR<cr/lf>
    j. 0MM<cr/lf>
    k. 0DS<cr/lf>
    l. 2SD<cr/lf>
    m. 3SC<cr/lf>
    n. 1BR<cr/lf>
    o. 0MM<cr/lf>
    p. 0DS<cr/lf>
    q. 2SD<cr/lf>
    r. 4SC<cr/lf>
    s. 1BR<cr/lf>
    t. 0MM<cr/lf>
    u. 0DS<cr/lf>
    v. 2SD<cr/lf>
    w. 0RC<cr/lf>
    x. 0RE<cr/lf>
2. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
    a. 1S<cr/lf>
    b. 0A<cr/lf>
    c. 40R<cr/lf>
    d. 3L+0x80+0x00+0x01+0x80+0x55+0x55+0x55+0x55+0x00+0x00+0x80+0x80<cr/lf>
    e. 0V<cr/lf>
    f. 1D<cr/lf>
    g. 1B<cr/lf>

3. Wait approximately 1 second they send the following commands to the Receiver.
   a. 1SC<cr/lf>
   b. 2SD<cr/lf>
4. Read back data from Channel 1 of the Receiver.
5. You will receive back the following six bytes:
   a. Binary hex 01,00,55,55,55,55
6. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 2SC<cr/lf>
   b. 2SD<cr/lf>
7. Read back data from Channel 2 of the Receiver.
   a. You will receive back the following six bytes:
   b. Binary hex 01,00,55,55,55,55
8. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   a. 3SC<cr/lf>
   b. 2SD<cr/lf>
9. Read back data from Channel 3 of the Receiver.
   a. You will receive back the following six bytes:
   b. Binary hex 01,00,55,55,55,55
10. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
    a. 4SC<cr/lf>
    b. 2SD<cr/lf>
11. Read back data from Channel 4 of the Receiver.
    a. You will receive back the following 6 bytes:
    b. Binary hex 01,00,55,55,55,55
12. Send the following command to the 73A-425 or Transmitter side of the VX4428:
    a. EX<cr/lf>
13. Read back data from the status command to the Receiver.
    a. You will receive the following three bytes:
    b. Binary Hex AA,0D,0A

Monitor Mode Interword Gap Error

1. Send the following commands to the 73A-426 or Receiver side of the VX4428:
   - **a.** RS<cr/lf>
   - **b.** 0TR<cr/lf>
   - **c.** 1SC<cr/lf>
   - **d.** 1BR<cr/lf>
   - **e.** 0MM<cr/lf>
   - **f.** 0DS<cr/lf>
   - **g.** 2SD<cr/lf>
   - **h.** 2SC<cr/lf>
   - **i.** 1BR<cr/lf>
   - **j.** 0MM<cr/lf>
   - **k.** 0DS<cr/lf>
   - **l.** 2SD<cr/lf>
   - **m.** 3SC<cr/lf>
   - **n.** 1BR<cr/lf>
   - **o.** 0MM<cr/lf>
   - **p.** 0DS<cr/lf>
   - **q.** 2SD<cr/lf>
   - **r.** 4SC<cr/lf>
   - **s.** 1BR<cr/lf>
   - **t.** 0MM<cr/lf>
   - **u.** 0DS<cr/lf>
   - **v.** 2SD<cr/lf>
   - **w.** 0RC<cr/lf>
   - **x.** 0RE<cr/lf>
2. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
   - **a.** 1S<cr/lf>
   - **b.** 0A<cr/lf>
   - **c.** 40R<cr/lf>
   - **d.** 4L+0x80+0x00+0x08+0x80+0x55+0x55+0x55+0x55+0x77+0x77+0x77+0x77+0x00+0x00+0x00+0x80+0x80<cr/lf>
   - **e.** 0V<cr/lf>
   - **f.** 1D<cr/lf>
   - **g.** 1B<cr/lf>
3. Wait approximately 1 second then send the following commands to the Receiver:
   - **a.** 1SC<cr/lf>
   - **b.** 2SD<cr/lf>

4. Read back data from Channel 1 of the Receiver.
   a. Look at the first two ARINC words.
   b. You will receive back the following 10 bytes:
   c. Binary hex 03,00,55,55,55,D5
   d. Binary hex 77,77,77,F7
5. Send the following commands to the Receiver:
   a. 2SC<cr/lf>
   b. 2SD<cr/lf>
6. Read back data from Channel 2 of the Receiver.
   a. Look at the first two ARINC words.
   b. You will receive back the following 10 bytes:
   c. Binary hex 03,00,55,55,55,D5
   d. Binary hex 77,77,77,F7
7. Send the following commands to the Receiver:
   a. 3SC<cr/lf>
   b. 2SD<cr/lf>
8. Read back data from Channel 3 of the Receiver.
   a. Look at the first two ARINC words.
   b. You will receive back the following 10 bytes:
   c. Binary hex 03,00,55,55,55,D5
   d. Binary hex 77,77,77,F7
9. Send the following commands to the Receiver:
   a. 4SC<cr/lf>
   b. 2SD<cr/lf>
10. Read back data from Channel 4 of the Receiver.
    a. Look at the first two ARINC words.
    b. You will receive back the following 10 bytes:
    c. Binary hex 03,00,55,55,55,D5
    d. Binary hex 77,77,77,F7
11. Send the following commands to the Receiver:
    a. EX<cr/lf>
12. Read back data from the status command to the Receiver.
    a. You will receive the following 3 bytes:
    b. Binary Hex AA,0D,0A

Monitor Mode 3/4 Memory Full Interrupt

1. Send the following commands to the 73A-426 or Receiver side of the VX4428:
   a. RS<cr/lf>
   b. 0TR<cr/lf>
   c. 1SC<cr/lf>
   d. 1BR<cr/lf>

e. 0MM<cr/lf>
f. 0DS<cr/lf>
g. 2SD<cr/lf>
h. 1IN<cr/lf>
i. 1RC<cr/lf>
j. 1RE<cr/lf>

2. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
a. 1S<cr/lf>
b. 0A<cr/lf>
c. 40R<cr/lf>
d. 4L+0x20,0x00,0x00,0x80,0x55,0x55,0x55,0x55,0x77,0x77,0x77,0x77,0x00,0x00,0x40, 0x80<cr/lf>
e. 0V<cr/lf>
f. 1D<cr/lf>
g. 1B<cr/lf>

3. Wait approximately 1 minute then see that the RXAFI light lights on the VX4428 or 73A-426.

4. Send a word serial Read STB command to the Receiver and read back FF71 then send a Interrupt acknowledge cycle to the Receiver.

5. Send the following command to the 73A-425 or Transmitter side of the VX4428:
a. 0Q<cr/lf>

6. Send the following commands to the 73A-426 or Receiver side of the VX4428:
a. RS<cr/lf>
b. 0TR<cr/lf>
c. 2SC<cr/lf>
d. 1BR<cr/lf>
e. 0MM<cr/lf>
f. 0DS<cr/lf>
g. 2SD<cr/lf>
h. 1IN<cr/lf>
i. 2RC<cr/lf>
j. 2RE<cr/lf>

7. Send the following command to the 73A-425 or Transmitter side of the VX4428:
a. 1B<cr/lf>

8. Wait approximately 1 minute then see that the RXAFI light lights on the VX4428 or 73A-426.

9. Send a word serial Read STB command to the Receiver and read back FF72 then send a Interrupt acknowledge cycle to the Receiver.

10. Send the following command to the 73A-425 or Transmitter side of the VX4428.
a. 0Q<cr/lf>

11. Send the following commands to the 73A-426 or Receiver side of the VX4428:
a. RS<cr/lf>
b. 0TR<cr/lf>

c. 3SC<cr/lf>
d. 1BR<cr/lf>
e. 0MM<cr/lf>
f. 0DS<cr/lf>
g. 2SD<cr/lf>
h. 1IN<cr/lf>
i. 3RC<cr/lf>
j. 3RE<cr/lf>

12. Send the following command to the 73A-425 or Transmitter side of the VX4428:
a. 1B<cr/lf>
13. Wait approximately 1 minute then see that the RXAFI light lights on the VX4428 or 73A-426.
14. Send a word serial Read STB command to the Receiver and read back FF74 then send a Interrupt acknowledge cycle to the Receiver.
15. Send the following command to the 73A-425 or Transmitter side of the VX4428.
a. 0Q<cr/lf>
16. Send the following commands to the 73A-426 or Receiver side of the VX4428:
a. RS<cr/lf>
b. 0TR<cr/lf>
c. 4SC<cr/lf>
d. 1BR<cr/lf>
e. 0MM<cr/lf>
f. 0DS<cr/lf>
g. 2SD<cr/lf>
h. 1IN<cr/lf>
i. 4RC<cr/lf>
j. 4RE<cr/lf>
17. Send the following command to the 73A-425 or Transmitter side of the VX4428:
a. 1B<cr/lf>
18. Wait approximately 1 minute then see that the RXAFI light lights on the VX4428 or 73A-426.
19. Send a word serial Read STB command to the Receiver and read back FF78 then send a Interrupt acknowledge cycle to the Receiver.

Limit Check Mode With Trigger Output

1. Connect Oscilloscope channel A to S2 pin 7. Set the scope to trigger one time on a negative edge at an amplitude of 2.00 V, time base set to 1.0 microseconds, and channel A amplitude set to 2.00 V.
2. Send the following commands to the 73A-426 or Receiver side of the VX4428:
a. RS<cr/lf>
b. 0TR<cr/lf>
c. 1SC<cr/lf>

d. 1BR<cr/lf>
e. 0DS<cr/lf>
f. 2MM<cr/lf>
g. SL+0X77+0X00
h. 2LP+0x77+0x77+0x78
i. 1PT<cr/lf>
j. 1TS+0x01+0x01
k. 13TE<cr/lf>
l. 0IN<cr/lf>
m. 1RC<cr/lf>
n. 1RE<cr/lf>

3. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
a. 1S<cr/lf>
b. 0A<cr/lf>
c. 40R<cr/lf>
d. 4L+0x20,0x00,0x00,0x80,0x77,0x77,0x77,0x79,0x77,0x77,0x77,0x77,0x00,0x00,0x40, 0x80<cr/lf>
e. 0V<cr/lf>
f. 1D<cr/lf>
g. 1B<cr/lf>

4. Wait approximately 50 milliseconds then send the following command to the 73A-426 or Receiver side of the VX4428.
a. EX<cr/lf>

5. Read back the status, you get a hex 0x01 returned. Channel A on the Oscilloscope will show a negative pulse approximately 1 microsecond wide at the 50% point.

6. Send the following command to the 73A-426 or Receiver side of the VX4428:
a. 0SD<cr/lf>

7. Read back the data word it will = 0x777777F7.

8. Send the following command to the 73A-425 or Transmitter side of the VX4428:
a. 0Q<cr/lf>

9. Send the following commands to the 73A-426 or Receiver side of the VX4428:
a. 1RD<cr/lf>
b. 2MM<cr/lf>
c. SL+0X77+0X00
d. 3LP+0x77+0x77+0x78
e. 1RE<cr/lf>

10. Send the following command to the 73A-425 or Transmitter side of the VX4428:
a. 1B<cr/lf>

11. Wait approximately 50 milliseconds then send the following command to the 73A-426 or Receiver side of the VX4428.
a. EX<cr/lf>

12. Read back the status, you get a hex 0x01 returned

13. Send the following command to the 73A-426 or Receiver side of the VX4428.

a. 0SD<cr/lf>

14. Read back the data word it will = 0x77777779.

15. Send the following command to the 73A-425 or Transmitter side of the VX4428:

a. 0Q<cr/lf>

16. Send the following commands to the 73A-426 or Receiver side of the VX4428:

a. 1RD<cr/lf>

b. 2MM<cr/lf>

c. SL+0X77+0X00

d. 1LP+0x77+0x77+0x78

e. 1RE<cr/lf>

17. Send the following command to the 73A-425 or Transmitter side of the VX4428:

a. 1B<cr/lf>

18. Wait approximately 50 milliseconds then send the following command to the 73A-426 or Receiver side of the VX4428.

a. EX<cr/lf>

19. Read back the status, you get a hex 0x00 returned. No interrupt.

20. Send the following command to the 73A-425 or Transmitter side of the VX4428:

a. 0Q<cr/lf>

21. Send the following commands to the 73A-426 or Receiver side of the VX4428:

a. RS<cr/lf>

b. 0TR<cr/lf>

c. 2SC<cr/lf>

d. 1BR<cr/lf>

e. 0DS<cr/lf>

f. 2MM<cr/lf>

g. SL+0X77+0X00

h. 2LP+0x77+0x77+0x78

i. 1PT<cr/lf>

j. 2TS+0x01+0x01

k. 23TE<cr/lf>

l. 0IN<cr/lf>

m. 2RC<cr/lf>

n. 2RE<cr/lf>

22. Send the following command to the 73A-425 or Transmitter side of the VX4428:

a. 1B<cr/lf>

23. Wait approximately 50 milliseconds then send the following command to the 73A-426 or Receiver side of the VX4428.

a. EX<cr/lf>

24. Read back the status, you get a hex 0x02 returned. Channel A on the Oscilloscope will show a negative pulse approximately 1 microsecond wide at the 50% point.

25. Send the following command to the 73A-426 or Receiver side of the VX4428:

a. 0SD<cr/lf>

26. Read back the data word it will = 0x777777F7.

27. Send the following command to the 73A-425 or Transmitter side of the VX4428:
- **a.** 0Q<cr/lf>

28. Send the following commands to the 73A-426 or Receiver side of the VX4428:
- **a.** 1RD<cr/lf>
- **b.** 2MM<cr/lf>
- **c.** SL+0X77+0X00
- **d.** 3LP+0x77+0x77+0x78
- **e.** 1RE<cr/lf>

29. Send the following command to the 73A-425 or Transmitter side of the VX4428:
- **a.** 1B<cr/lf>

30. Wait approximately 50 milliseconds then send the following command to the 73A-426 or Receiver side of the VX4428.
- **a.** EX<cr/lf>

31. Read back the status, you get a hex 0x02 returned

32. Send the following command to the 73A-426 or Receiver side of the VX4428:
- **a.** 0SD<cr/lf>

33. Read back the data word it will = 0x77777779.

34. Send the following command to the 73A-425 or Transmitter side of the VX4428:
- **a.** 0Q<cr/lf>

35. Send the following commands to the 73A-426 or Receiver side of the VX4428:
- **a.** 1RD<cr/lf>
- **b.** 2MM<cr/lf>
- **c.** SL+0X77+0X00
- **d.** 1LP+0x77+0x77+0x78
- **e.** 1RE<cr/lf>

36. Send the following command to the 73A-425 or Transmitter side of the VX4428:
- **a.** 1B<cr/lf>

37. Wait approximately 50 milliseconds then send the following command to the 73A-426 or Receiver side of the VX4428:
- **a.** EX<cr/lf>

38. Read back the status, you get a hex 0x00 returned. No interrupt.

39. Send the following command to the 73A-425 or Transmitter side of the VX4428:
- **a.** 0Q<cr/lf>

40. Send the following commands to the 73A-426 or Receiver side of the VX4428:
- **a.** RS<cr/lf>
- **b.** 0TR<cr/lf>
- **c.** 3SC<cr/lf>
- **d.** 1BR<cr/lf>
- **e.** 0DS<cr/lf>
- **f.** 2MM<cr/lf>
- **g.** SL+0X77+0X00
- **h.** 2LP+0x77+0x77+0x78

i. 1PT<cr/lf>
j. 3TS+0x01+0x01
k. 33TE<cr/lf>
l. 0IN<cr/lf>
m. 3RC<cr/lf>
n. 3RE<cr/lf>

41. Send the following command to the 73A-425 or Transmitter side of the VX4428:
a. 1B<cr/lf>

42. Wait approximately 50 milliseconds then send the following command to the 73A-426 or Receiver side of the VX4428.
a. EX<cr/lf>

43. Read back the status, you get a hex 0x10 returned. Channel A on the Oscilloscope will show a negative pulse approximately 1 microsecond wide at the 50% point.

44. Send the following command to the 73A-426 or Receiver side of the VX4428:
a. 0SD<cr/lf>

45. Read back the data word it will = 0x777777F7.

46. Send the following command to the 73A-425 or Transmitter side of the VX4428:
a. 0Q<cr/lf>

47. Send the following commands to the 73A-426 or Receiver side of the VX4428:
a. 1RD<cr/lf>
b. 2MM<cr/lf>
c. SL+0X77+0X00
d. 3LP+0x77+0x77+0x78
e. 1RE<cr/lf>

48. Send the following command to the 73A-425 or Transmitter side of the VX4428:
a. 1B<cr/lf>

49. Wait approximately 50 milliseconds then send the following command to the 73A-426 or Receiver side of the VX4428:
a. EX<cr/lf>

50. Read back the status, you get a hex 0x10 returned

51. Send the following command to the 73A-426 or Receiver side of the VX4428:
a. 0SD<cr/lf>

52. Read back the data word it will = 0x77777779.

53. Send the following command to the 73A-425 or Transmitter side of the VX4428:
a. 0Q<cr/lf>

54. Send the following commands to the 73A-426 or Receiver side of the VX4428.
a. 1RD<cr/lf>
b. 2MM<cr/lf>
c. SL+0X77+0X00
d. 1LP+0x77+0x77+0x78
e. 1RE<cr/lf>

55. Send the following command to the 73A-425 or Transmitter side of the VX4428:
a. 1B<cr/lf>

56. Wait approximately 50 milliseconds then send the following command to the 73A-426 or Receiver side of the VX4428:
- **a.** EX<cr/lf>

57. Read back the status, you get a hex 0x00 returned. No interrupt.

58. Send the following command to the 73A-425 or Transmitter side of the VX4428:
- **a.** 0Q<cr/lf>

59. Send the following commands to the 73A-426 or Receiver side of the VX4428:
- **a.** RS<cr/lf>
- **b.** 0TR<cr/lf>
- **c.** 4SC<cr/lf>
- **d.** 1BR<cr/lf>
- **e.** 0DS<cr/lf>
- **f.** 2MM<cr/lf>
- **g.** SL+0X77+0X00
- **h.** 2LP+0x77+0x77+0x78
- **i.** 1PT<cr/lf>
- **j.** 4TS+0x01+0x01
- **k.** 43TE<cr/lf>
- **l.** 0IN<cr/lf>
- **m.** 4RC<cr/lf>
- **n.** 4RE<cr/lf>

60. Send the following command to the 73A-425 or Transmitter side of the VX4428:
- **a.** 1B<cr/lf>

61. Wait approximately 50 milliseconds then send the following command to the 73A-426 or Receiver side of the VX4428:
- **a.** EX<cr/lf>

62. Read back the status, you get a hex 0x40 returned. Channel A on the Oscilloscope will show a negative pulse approximately 1 microsecond wide at the 50% point.

63. Send the following command to the 73A-426 or Receiver side of the VX4428:
- **a.** 0SD<cr/lf>

64. Read back the data word it will = 0x777777F7.

65. Send the following command to the 73A-425 or Transmitter side of the VX4428:
- **a.** 0Q<cr/lf>

66. Send the following commands to the 73A-426 or Receiver side of the VX4428:
- **a.** 1RD<cr/lf>
- **b.** 2MM<cr/lf>
- **c.** SL+0X77+0X00
- **d.** 3LP+0x77+0x77+0x78
- **e.** 1RE<cr/lf>

67. Send the following command to the 73A-425 or Transmitter side of the VX4428:
- **a.** 1B<cr/lf>

68. Wait approximately 50 milliseconds then send the following command to the 73A-426 or Receiver side of the VX4428:
   a. EX<cr/lf>
69. Read back the status, you get a hex 0x40 returned
70. Send the following command to the 73A-426 or Receiver side of the VX4428:
   a. 0SD<cr/lf>
71. Read back the data word it will = 0x77777779.
72. Send the following command to the 73A-425 or Transmitter side of the VX4428:
   a. 0Q<cr/lf>
73. Send the following commands to the 73A-426 or Receiver side of the VX4428:
   a. 1RD<cr/lf>
   b. 2MM<cr/lf>
   c. SL+0X77+0X00
   d. 1LP+0x77+0x77+0x78
   e. 1RE<cr/lf>
74. Send the following command to the 73A-425 or Transmitter side of the VX4428:
   a. 1B<cr/lf>
75. Wait approximately 50 milliseconds then send the following command to the 73A-426 or Receiver side of the VX4428.
   a. EX<cr/lf>
76. Read back the status, you will get a hex 0x00 returned with no interrupt.
77. Send the following command to the 73A-425 or Transmitter side of the VX4428:
   a. 0Q<cr/lf>

Receiver Amplitude Test

1. Send the following commands to the 73A-426 or Receiver side of the VX4428:
   a. RS<cr/lf>
   b. 0TR<cr/lf>
   c. 1SC<cr/lf>
   d. 1BR<cr/lf>
   e. 0MM<cr/lf>
   f. 0DS<cr/lf>
   g. 2SC<cr/lf>
   h. 1BR<cr/lf>
   i. 0MM<cr/lf>
   j. 0DS<cr/lf>
   k. 3SC<cr/lf>
   l. 1BR<cr/lf>
   m. 0MM<cr/lf>
   n. 0DS<cr/lf>
   o. 4SC<cr/lf>

p. 1BR<cr/lf>
q. 0MM<cr/lf>
r. 0DS<cr/lf>
s. 0RC<cr/lf>
t. 0RE<cr/lf>

2. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
a. 1S<cr/lf>
b. 0A<cr/lf>
c. 40R<cr/lf>
d. 4L+0x20+0x00+0x00+0x80+0x55+0x55+0x55+0x55+0x77+0x77+0x77+0x77+0x00+0x00+0x00+0x80+0x80<cr/lf>
e. 2V<cr/lf>
f. 1D<cr/lf>
g. 1B<cr/lf>

3. Wait approximately 50 milliseconds then send the following commands to the Receiver:
a. 1SC<cr/lf>
b. 2SD<cr/lf>

4. Read back data from Channel 1 of the Receiver.
a. Look at the first two ARINC words.
b. You will receive back the following 10 bytes:
c. Binary hex 02,00,55,55,55,D5
d. Binary hex 77,77,77,F7

5. Send the following commands to the Receiver:
a. 2SC<cr/lf>
b. 2SD<cr/lf>

6. Read back data from Channel 1 of the Receiver.
a. Look at the first two ARINC words.
b. You will receive back the following 10 bytes:
c. Binary hex 02,00,55,55,55,D5
d. Binary hex 77,77,77,F7

7. Send the following commands to the Receiver:
a. 3SC<cr/lf>
b. 2SD<cr/lf>

8. Read back data from Channel 1 of the Receiver.
a. Look at the first two ARINC words.
b. You will receive back the following 10 bytes:
c. Binary hex 02,00,55,55,55,D5
d. Binary hex 77,77,77,F7

9. Send the following commands to the Receiver:
a. 4SC<cr/lf>
b. 2SD<cr/lf>

10. Read back data from Channel 1 of the Receiver.
- **a.** Look at the first two ARINC words.
- **b.** You will receive back the following 10 bytes:
- **c.** Binary hex 02,00,55,55,55,D5
- **d.** Binary hex 77,77,77,F7

11. Send the following command to the Receiver:
- **a.** 0RD<cr/lf>

12. Send the following commands to the 73A-425 or Transmitter side of the VX4428:
- **a.** 0Q<cr/lf>
- **b.** 3V<cr/lf>

13. Send the following command to the Receiver:
- **a.** 0RE<cr/lf>

14. Send the following command to the 73A-425 or Transmitter side of the VX4428:
- **a.** 1B<cr/lf>

15. Wait approximately 50 milliseconds then send the following commands to the Receiver:
- **a.** 1SC<cr/lf>
- **b.** 2SD<cr/lf>

16. Read back data from Channel 1 of the Receiver.
- **a.** Look at the first two ARINC words.
- **b.** You will receive back the following 2 bytes:
- **c.** Binary hex 00,00

17. Send the following commands to the Receiver:
- **a.** 2SC<cr/lf>
- **b.** 2SD<cr/lf>

18. Read back data from Channel 1 of the Receiver.
- **a.** Look at the first two ARINC words.
- **b.** You will receive back the following 2 byte:
- **c.** Binary hex 00,00

19. Send the following commands to the Receiver:
- **a.** 3SC<cr/lf>
- **b.** 2SD<cr/lf>

20. Read back data from Channel 1 of the Receiver.
- **a.** Look at the first two ARINC words.
- **b.** You will receive back the following 2 byte:
- **c.** Binary hex 00,00

21. Send the following commands to the Receiver:
- **a.** 4SC<cr/lf>
- **b.** 2SD<cr/lf>

22. Read back data from Channel 1 of the Receiver.
- **a.** Look at the first two ARINC words.
- **b.** You will receive back the following 2 byte:
- **c.** Binary hex 00,00

23. Send the following command to the Receiver:
   a. 0RD<cr/lf>
24. Send the following command to the 73A-425 or Transmitter side of the VX4428:
   a. 0Q<cr/lf>